4-MEGAPIXEL CMOS ACTIVE-PIXEL DIGITAL IMAGE SENSOR

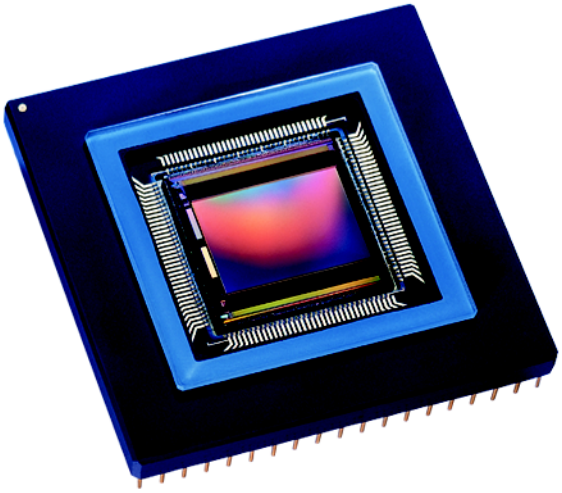
MI-MV40

Micron Part Number: MT9M440C36ST

Description

The MI-MV40 is a 2,352H x 1,728V (4-megapixel) CMOS digital image sensor capable of 200-frames-per-second (fps) operation. Available in monochrome or color, it has on-chip, 10-bit analog-to-digital converters (ADCs), which are self-calibrating, and a fully digital input interface. The chip's input clock rate is 50 MHz at 200 fps, providing compatibility with many off-the-shelf interface components.

The sensor has sixteen 10-bit-wide column-parallel digital output ports. Its open architecture provides access to internal operations. ADC timing and pixel-read control are integrated on-chip. At 200 fps, the sensor dissipates <700mW. It operates on a 3.3V supply. Pixel size is 7 microns square, and digital responsivity is about 2,500 bits per lux-second.



Features

- Array Format: 2,352H x 1,728V (4,064,256 pixels)
- Aspect Ratio: 4:3
- Pixel Size and Type: 7.0µm x 7.0µm active-pixel photodiode
- Sensor Imaging Area: H: 16.46mm, V: 12.10mm, Diagonal: 20.43mm
- Frame Rate: 0–200+ fps, progressive-scan
- Output Data Rate: 975 Mb/s (200 fps)
- Power Consumption: <700mW @ 200 fps (data dependent)
- Digital Responsivity: Monochrome 2,500 bits per lux-second @ 550nm; ADC reference @ 1V
- Internal Intra-Scene Dynamic Range: 59dB
- Supply Voltage: +3.3V
- Operating Temperature: -5°C to +60°C
- Output: 10-bit digital through 16 parallel ports
- Color: Monochrome or color (Bayer RGB)
- Shutter: Electronic rolling shutter (ERS)
- ADC: On-chip 10-bit column-parallel
- Package: 280-pin ceramic PGA
- Programmable Controls: Open architecture

On-chip:

- Basic ADC controls
- Output multiplexing control
- ADC calibration

Off-chip:

- Multiple windowing
- Window size and location
- Electronic pan and tilt
- Frame rate and data rate
- Integration time
- ADC reference
- Read/write ADC calibration coefficients

General

The MI-MV40 CMOS image sensor has an open architecture to provide access to its internal operations. A complete camera system can be built by using the chip in conjunction with the following external devices:

- An FPGA/CPLD/ASIC controller, to manage the timing signals needed for sensor operation.
- A 1-inch lens.
- Biasing circuits and bypass capacitors.

Figure 1: A Camera System using the MI-MV40 CMOS Image Sensor

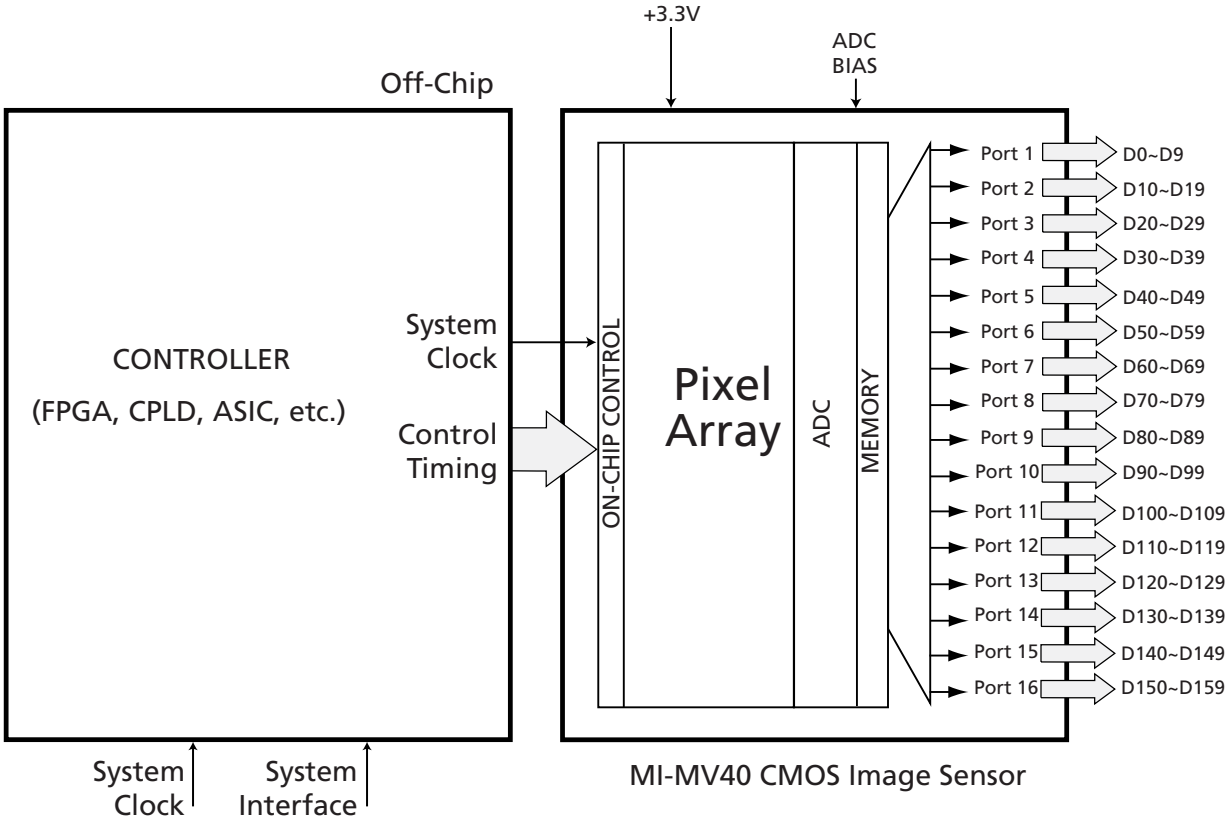


Figure 2: Sensor Architecture

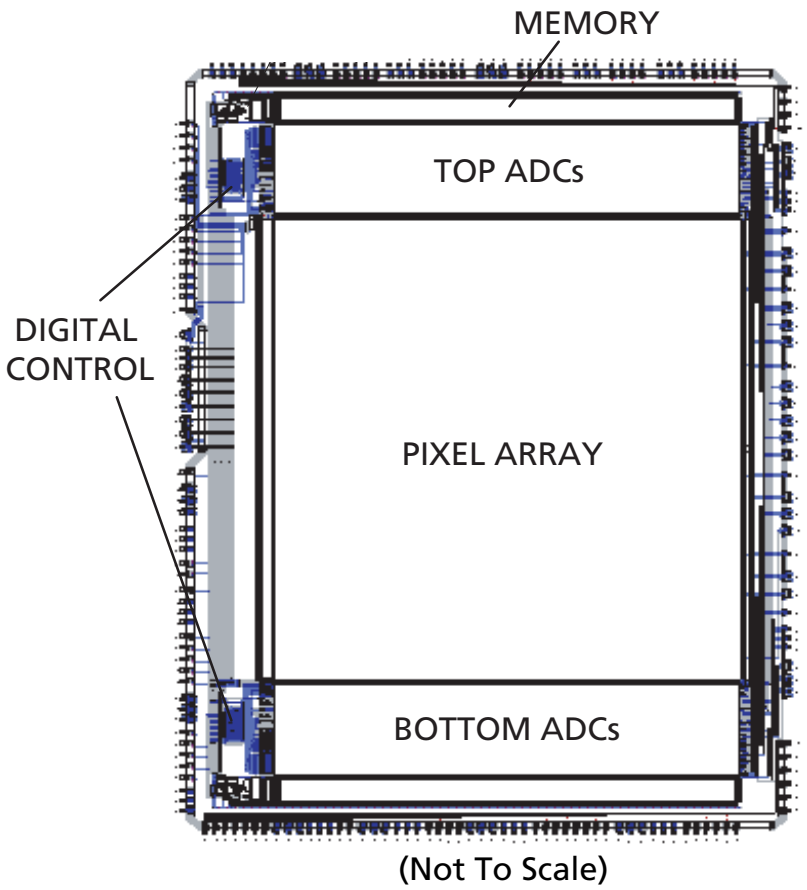


Figure 3: Signal Path Diagram

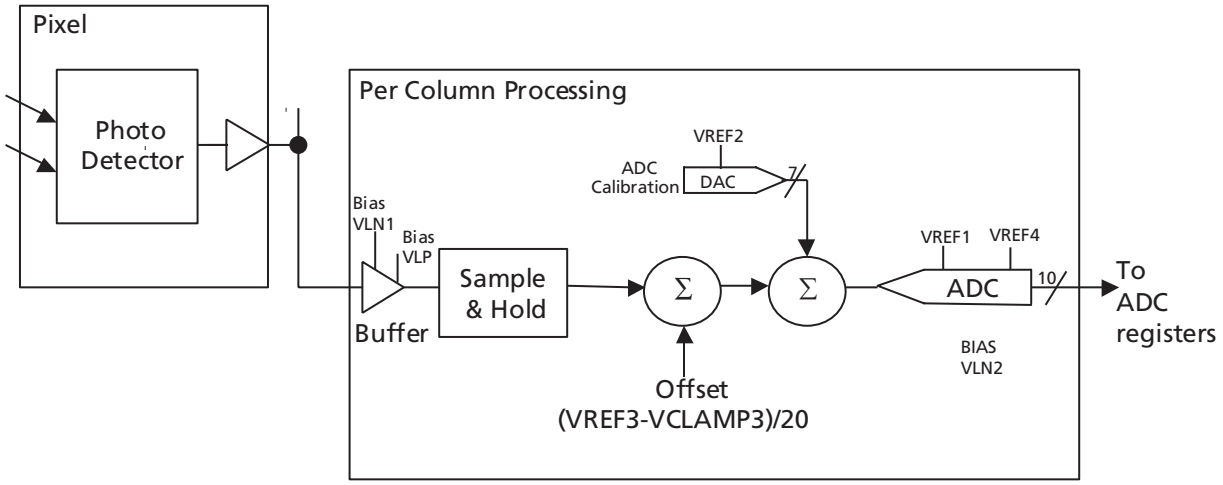
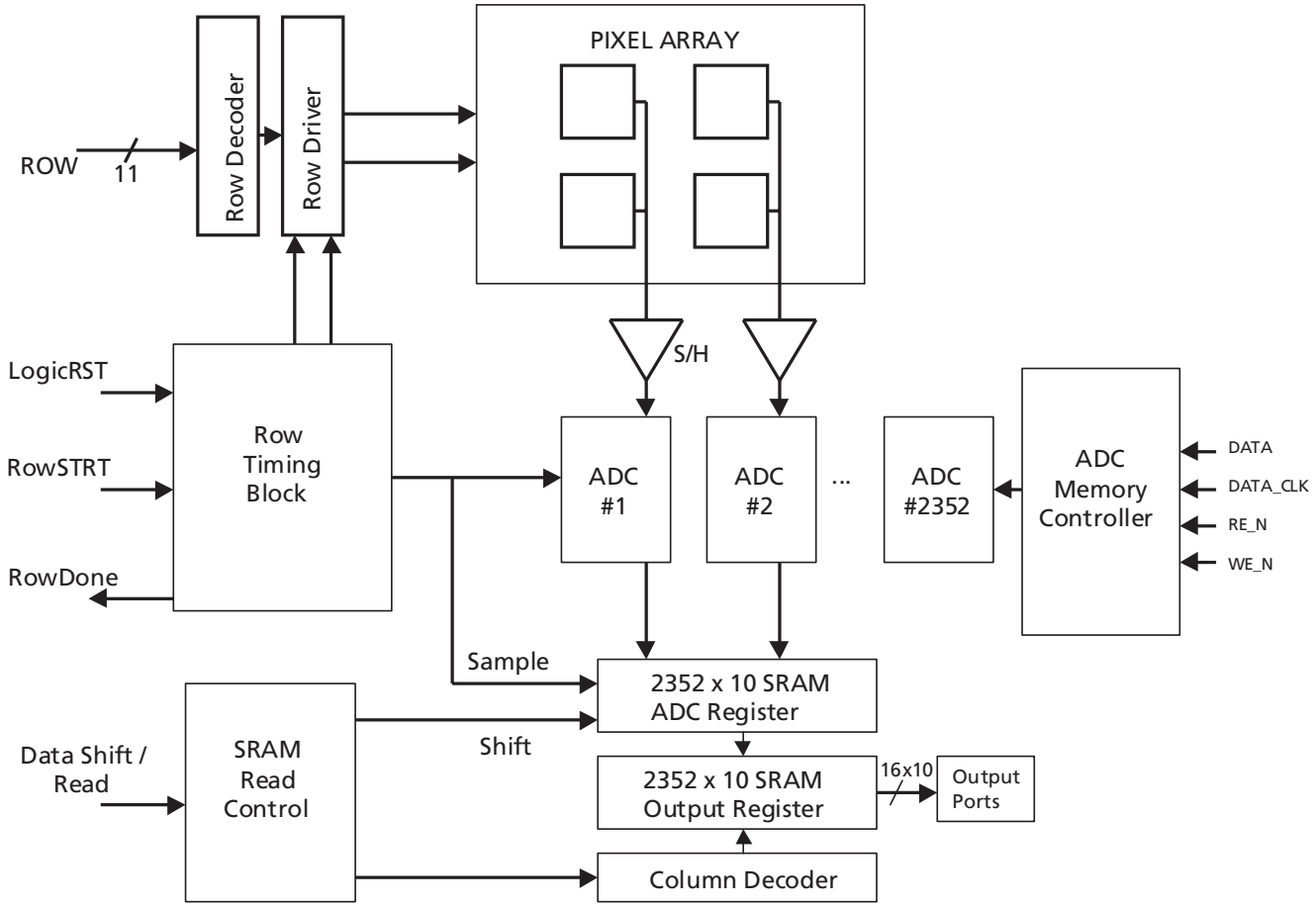


Figure 4: Functional Block Diagram



External Control Sequence

The MI-MV40 includes on-chip timing and control circuitry to control most of the pixel, ADC, and output multiplexing operations. However, the sensor still requires a controller (FPGA, CPLD, ASIC, etc.) to guide it through the full sequence of its operation.

The sensor has a column-parallel ADC architecture that allows the array of 2,352 analog-to-digital converters on the chip to digitize simultaneously the analog data from an entire pixel row. The following input signals are utilized to control the conversion and readout process:

Table 1: Conversion And Readout Process

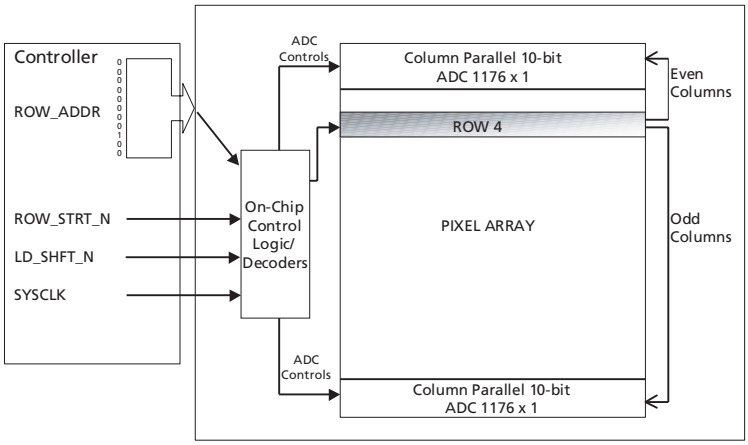
SIGNAL NAME	DESCRIPTION	INPUT BUS WIDTH
ROW_ADDR	Row Address	11-bit
ROW_STRT_N	Row Start	1-bit
LD_SHFT_N	Load shift register	1-bit
DATA_READ_EN_N	Data read enable	1-bit

The 11-bit ROW_ADDR (row address) input bus selects the pixel row to be read for each readout cycle. The ROW_STRT_N signal starts the process of reading the analog data from the pixel row, the analog-to-digital conversion, and the storage of the digital values in the ADC registers. When these actions are completed, the sensor sends a response back to the system controller using the ROW_DONE_N. Row address must be valid for the first half of the row processing time (the period between ROW_START_N and ROW_DONE_N).

The MI-MV40 contains a pipeline style memory array, which is used to store the data after digitization. This memory also allows the data from the previous row conversion cycle to be read while a new conversion is taking place.

The digital readout is controlled by lowering the LD_SHFT_N signal. LD_SHFT_N transfers the digitized data from the ADC register to the output register. DATA_READ_EN_N is used to enable the data output from the output register. DATA_READ_EN_N can be kept low (enabled) if the user does not want to skip output data. The output register allows the reading of the digital data from the previous row to be performed at the same time as a new conversion (pipeline mode). This means that the total row time will be only that between when: (a) the ROW_STRT_N signal is applied and ROW_DONE_N is returned; and (b) LD_SHFT_N is applied. The pipelined operation means there will always be 1 row of latency at the start of sensor operation. The alternative to pipeline mode is sequential mode in which a new pixel row conversion is not initiated until after the output register is emptied (and LD_SHFT_N has been taken high). The ratio of line active and blanking times can be adjusted to easily match a variety of display and collection formats.

Figure 5: Example 1 - This Example Shows Row 4 Being Digitized



1. Reads the contents of pixel row specified by ROW_ADDR
2. Converts pixel row signals to digital values
3. Stores digital values in ADC register (2352 x 10 bit)

ROW_ADDR

The address for the pixel row to be read is input externally via this 11-bit input bus. Addresses above 1728 are invalid. Must be valid for at least 50 SYSCLK cycles, must be valid when ROW_STRT_N is pulled low or can be changed simultaneously with the lowering of ROW_STRT_N.

ROW_STRT_N

This signal reads the contents of the pixel row specified by ROW_ADDR, converts pixel row signal to digital value, stores digital value in ADC register (2352 x 10-bit), and resets the pixel row. Must be valid for a minimum of two clock cycles. Should be returned high before ROW_DONE_N goes low.

ROW_DONE_N

127 SYSCLK cycles after ROW_STRT_N has been pulled low the sensor acknowledges the completion of a row read operation/digitization by sending out a low going pulse on this pin. Valid for two clock cycles.

LD_SHFT_N

This signal transfers the digitized data from the ADC register to the output register (2352 x 10-bit) and gates the power to the sense amplifiers. The first data (columns 1-16) are available for output at the third rising edge of SYSCLK after LD_SHFT_N is pulled low. May be enabled simultaneously with or after the falling edge of ROW_DONE_N. Must remain low the entire time the data is being read out.

DATA_READ_EN_N

This signal is used to enable the data output from the output register (2352 x 10-bit) to the sixteen, 10-bit output ports. May be initiated simultaneously with or after LD_SHFT_N is selected. This control can always be low.

Pixel Array

The pixel array of the MI-MV40 image sensor is vertically partitioned into 147 groups of 16 columns that correspond to the sensor's sixteen (16) identical output ports.The first column of each 16-column set always goes to Port 1, while the last column of each set goes to Port 16, etc. The operator can access all pixels of the MI-MV40 only by using all of its ports.

Table 2: Pixel Array Addresses

PORT	CLK 1	CLK 2	. . .	CLK147
Port 1	Col. 1	Col. 17		Col. 2337
Port 2	Col. 2	Col. 18		Col. 2338
Port 3	Col. 3	Col. 19		Col. 2339
Port 4	Col. 4	Col. 20		Col. 2340
Port 5	Col. 5	Col. 21		Col. 2341
Port 6	Col. 6	Col. 22		Col. 2342
Port 7	Col. 7	Col. 23		Col. 2343
Port 8	Col. 8	Col. 24		Col. 2344
Port 9	Col. 9	Col. 25		Col. 2345
Port 10	Col. 10	Col. 26		Col. 2346
Port 11	Col. 11	Col. 27		Col. 2347
Port 12	Col. 12	Col. 28		Col. 2348
Port 13	Col. 13	Col. 29		Col. 2349
Port 14	Col. 14	Col. 30		Col. 2350
Port 15	Col. 15	Col. 31		Col. 2351
Port 16	Col. 16	Col. 32		Col. 2352

Output Register

The use of an output register allows the processing of a row to be performed while the digital data from the previous operation is being read out of the sensor. A new pixel readout and conversion cycle can be started when LD_SHFT_N is pulled low.

Detail timing for one row is presented on the next page. In full horizontal resolution mode one row should last for a minimum of 152 SYSCLK cycles. However, in lower resolution modes such as 2048x1536 or less, data readout can be stopped (LD_SHFT_N and DATA_READ_EN_N returned high) after 132 SYSCLK cycles. This is the minimum row time in terms of clock cycles needed to complete row operations.

Figure 6: Timing Diagram For One Row

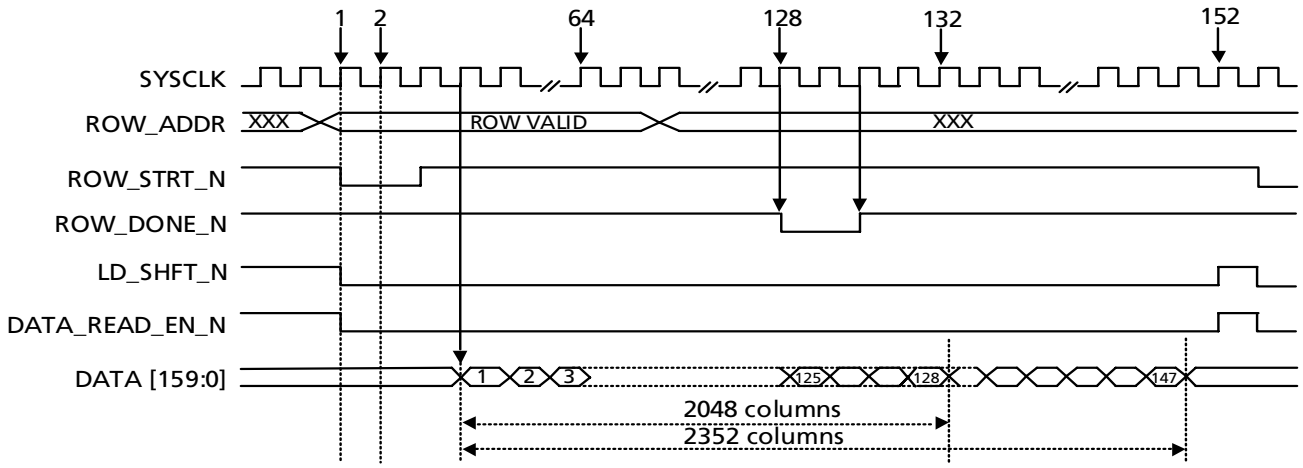
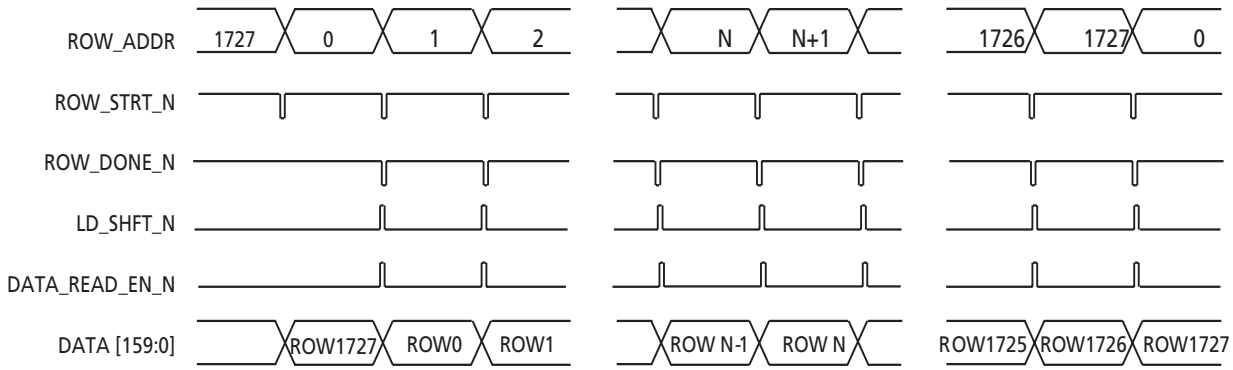
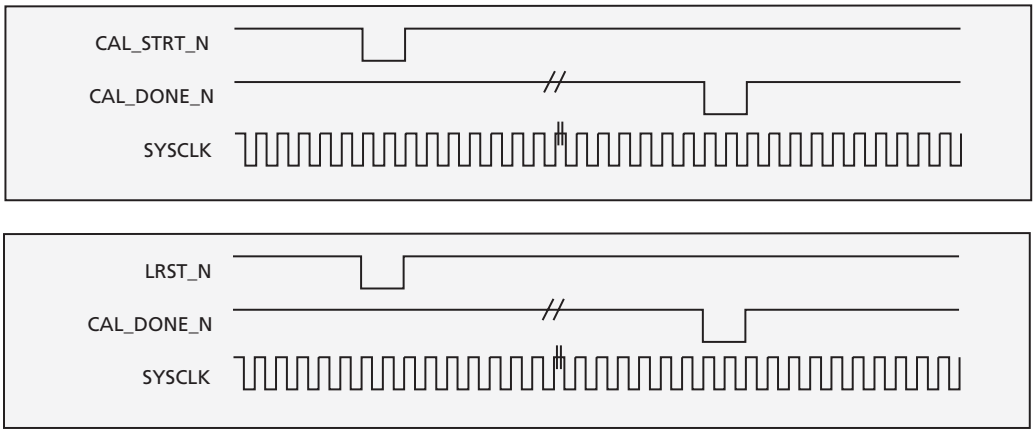


Figure 7: Frame Timing



The MI-MV40 contains special self-calibrating circuitry that enables it to reduce its own column-wise fixed-pattern noise. This calibration process consists of connecting a calibration signal (VREF2) to each of the ADC inputs, and estimating and storing these offsets (7 bits) to subtract from subsequent samples. The Typical I/O Signal Timing (Initialization Sequence) diagram shows the timing sequence to calibrate the sensor. Calibration occurs automatically after logic reset (LRST_N) but it can also be started by the user, by pulling CAL_STRT_N low. When calibration is finished, the sensor generates the active low CAL_DONE_N. Significant ambient temperature drift may justify re-calibration.

Figure 8: Typical I/O Signal Timing (Initialization Sequence)



CAL_STRT_N

CAL_STRT_N is a two-clock cycle-wide active-low pulse that initiates the ADC calibration sequence. The pulse must not be actuated for 1 microsecond after either power-up or removal of the sensor from a power-down state. Users may find it easiest to calibrate by means of the logic reset. The user should ensure that all analog biases are settled prior to initiating a calibration sequence.

CAL_DONE_N

CAL_DONE_N is a two-clock cycle-wide active-low output pulse that is asserted when the ADC calibration is complete. The device will automatically initiate a calibration sequence upon a logic reset. Completion of this sequence, in cases where it is initiated by a reset, is still with the CAL_DONE_N signal. This process is complete within 254 SYSCLK cycles of CAL_STRT_N. This process is complete within 254 SYSCLK cycles of LRST_N.

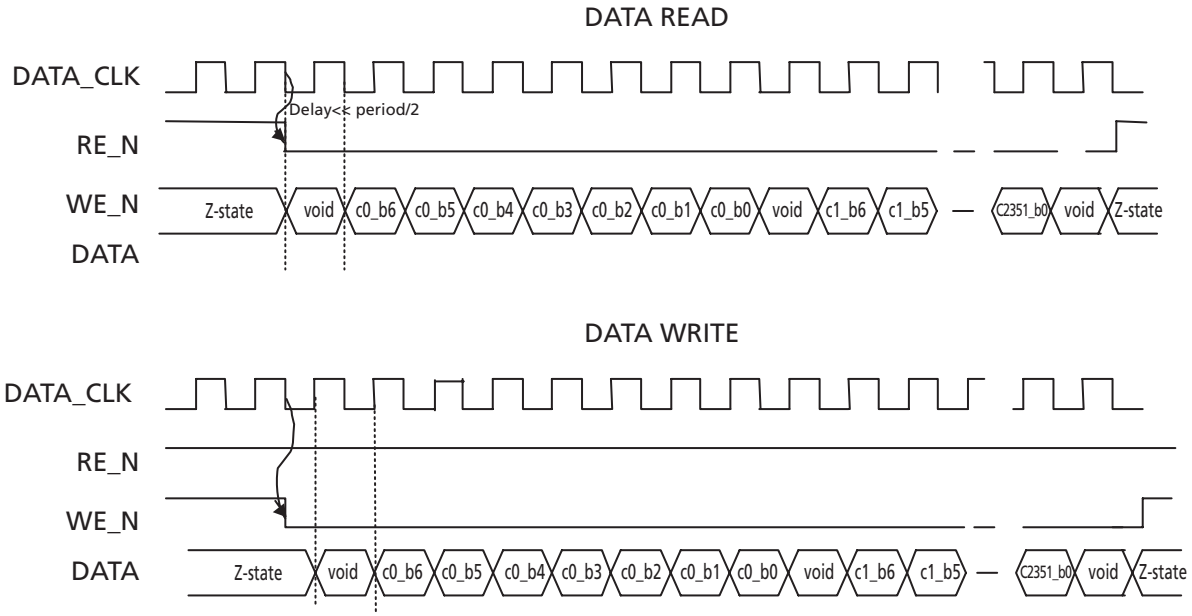
LRST_N

LRST_N is a two-clock cycle-wide active-low pulse that resets the digital logic. It puts all logic into a known state (all flip-flops are reset). This signal also initiates an ADC calibration sequence.

While row controller is busy (performs the operations after “start row” or calibration commands) it is insensitive to a new ROW_STRT_N or CAL_STRT_N pulse.

The chip also has an external read/write access to the ADC calibration values. The ADC calibration values are stored in SRAM as 7-bit digital numbers which are used to drive 7-bit DACs. Using the four-pin serial interface the user can access calibration data, read them out, optimize and write back. The interface protocol is defined in 9. Recommended frequency of the serial interface clock is 1 MHz.

Figure 9: ADC Calibration SRAM Write-Read Convention



NOTE: c0_b6 = column 0 bit 6 (bit6= DAC MSB); ADCs from 0 to 2351

Electronic Shutter

The MI-MV40 utilizes an ERS. To understand the ERS some key points must be kept in mind. First, referring back to "External Control Sequence" on page 5, recall that each time a row is selected (e.g., ROW_ADDR and ROW_STRT_N are applied) all the pixels in the row are read and reset. The read operation ends integration for the selected row and the reset operation defines the start of the next exposure. The integration time for a given row is the time between successive resets and reads for that row.

Secondly, it should be noted that the MI-MV40 has a fast rolling reset mode (enabled with ROL_RST) in which each time a row is selected (e.g., ROW_ADDR and ROW_STRT_N are applied) in addition to the first read and reset there is a second reset allowed for a second row. This essentially allows a doubling of the read/reset sequence in some instances because one row is readout and a second row is reset during a single row processing time.

ERS Mode with Exposure Greater than Frame Time (Single Pointer for READ and RESET)

The MI-MV40 can be operated in an ERS mode to control the sensor integration time. When the user wishes to select an integration time that is equal to or exceeds the frame time (i.e., frame readout time), a single READ and RESET POINTER is used to read data from and reset each row of pixels, as shown in 10.

RESET POINTER and READ POINTER are not signals generated by the sensor but rather user-generated constructs utilized here to illustrate the ERS concept.

This is done by changing the row address using ROW_ADDR to point to the appropriate row on the sensor. In a typical application, a sequence of rows is read out repeatedly. The integration time of a row is set by the time elapsed between successive selection of a particular row (a row is selected using the ROW_ADDR and pulsing ROW_STRT_N), as shown in 11. Please recall that ROW_STRT_N both reads and resets the row specified by ROW_ADDR. The integration time is simply the inverse of the frame rate (i.e. 60fps @16 msec integration time) in this mode. At system power-up the user should move the READ and RESET POINTER, along the pixel array, row by row, to reset all pixels and start integration.

Figure 10: ERS With a Single Pointer For READ or RESET

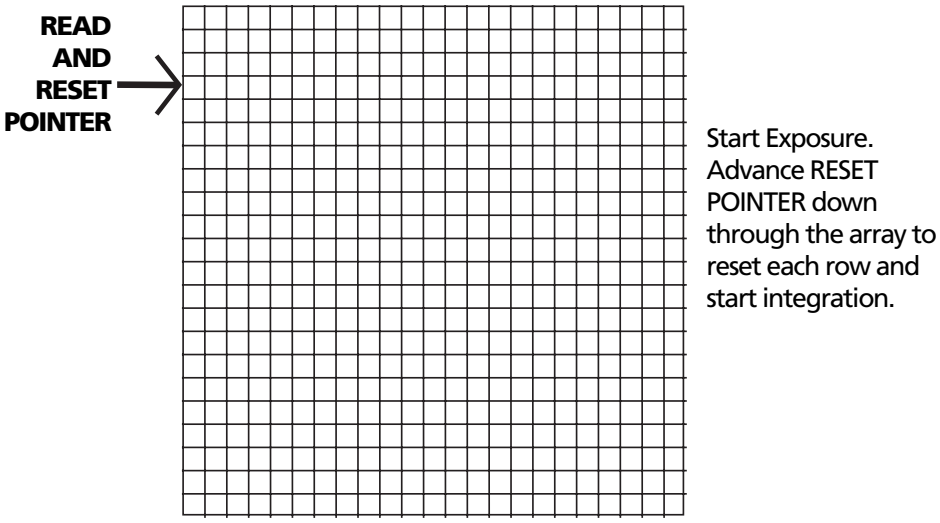


Figure 11: Reading a Window of 5 Rows with a Single READ and RESET Pointer

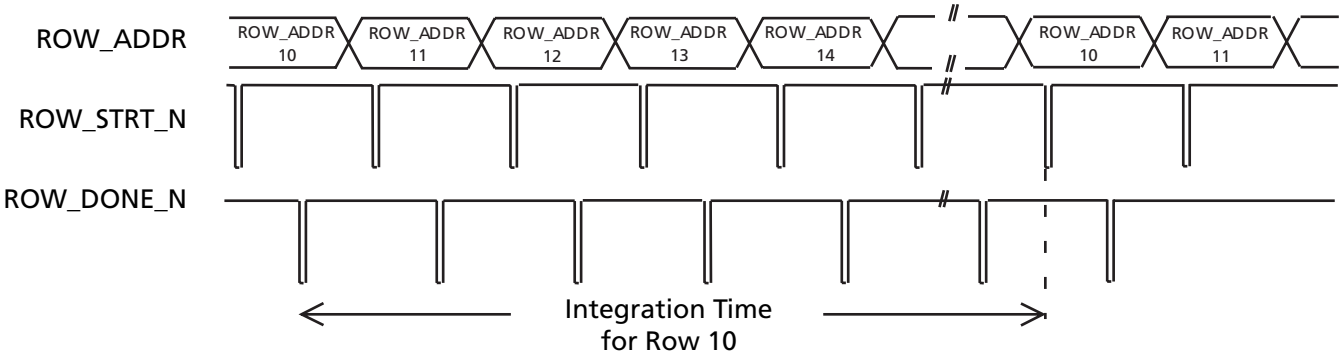
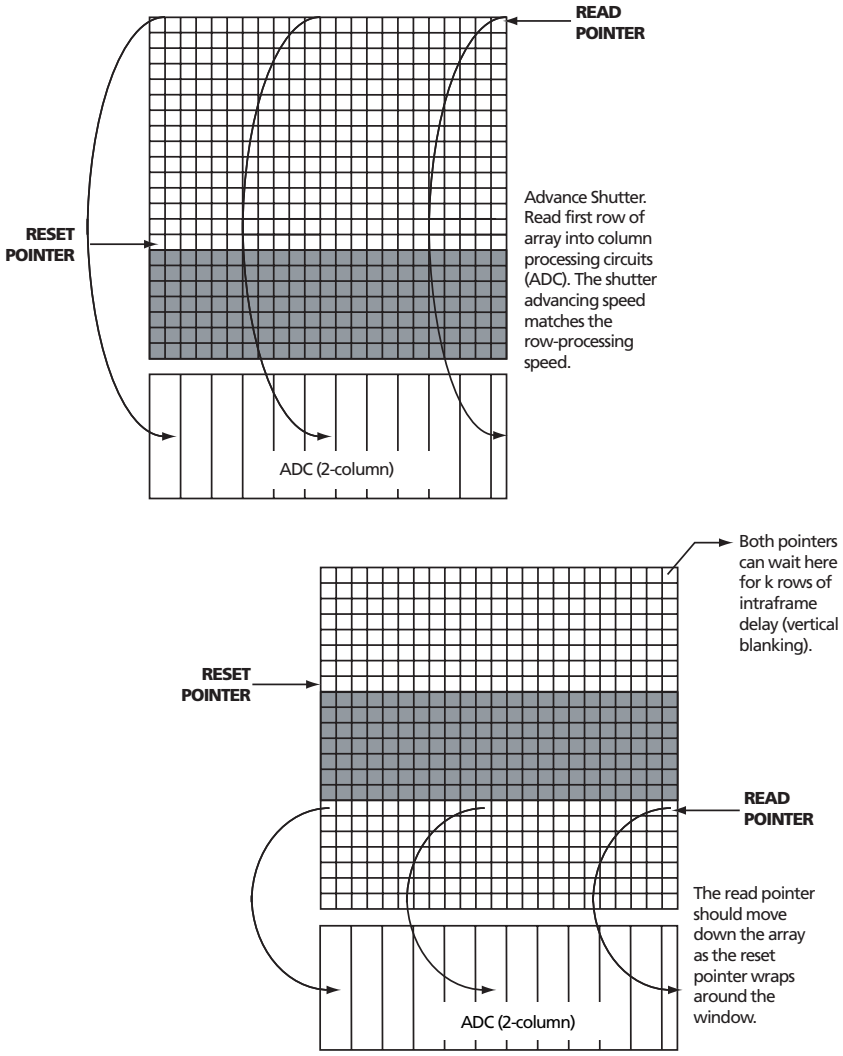


Figure 12: ERS with Dual RESET and READ Pointers

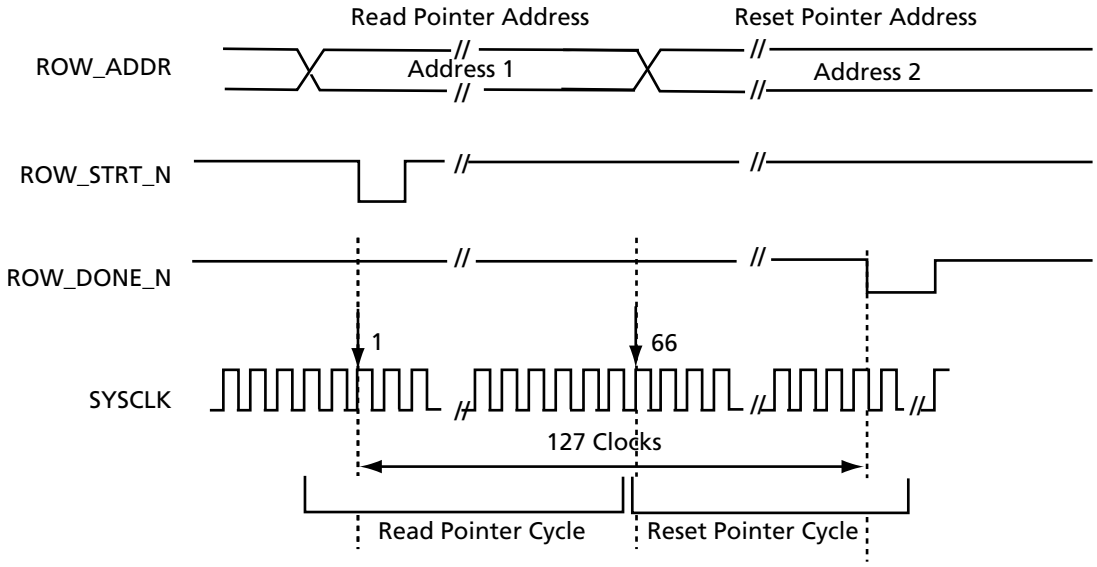


ERS Mode with Exposure Less than Frame Time (Dual READ and RESET Pointers)

When the user wishes to select an integration time that is less than the frame time, separate pointers can be used for reading a row and resetting a row. The user can still use the ROW_STRT_N pulse to initiate both row read and row reset. However, using ROW_STRT_N to initiate reset only is not time efficient because it causes two address pointers to be used on each row cycle, thus the effective frame rate is two times less compared to full-frame integration mode. An efficient way to reset rows is through the use of the ROL_RST control. When this input is HIGH, pixel reset appears twice during row time, the first time during row readout sequence (clocks 1-66), and the second time during clocks 66-128. It is recommended that the user change the address from the read address to the reset address at the 66th clock. When the address is switched from the current row read address to the current row reset address the selected row gets reset (without read and ADC conversion) to start a new integration. Both of these address pointers are controlled by the user-supplied ROW_ADDR input. In each row cycle, the first address (READ POINTER) is used to read data from a row. The second address (RESET POINTER) is used only to reset another row. This sets the starting point of integration for that row. The row read by the READ POINTER had been reset by the RESET POINTER during a previous cycle. The difference between the value of the READ POINTER and the RESET POINTER sets the integration time, as shown in12. After system power-up, the user should move the RESET POINTER along the pixel array, row by row, while the READ POINTER stays in place. When the RESET POINTER reaches the desired row number and integration time, the READ POINTER should start moving along the pixel array. When the READ POINTER reaches the bottom (last row) of the pixel array, it should wrap around and go back to the top. The RESET POINTER should never catch up with the READ POINTER.

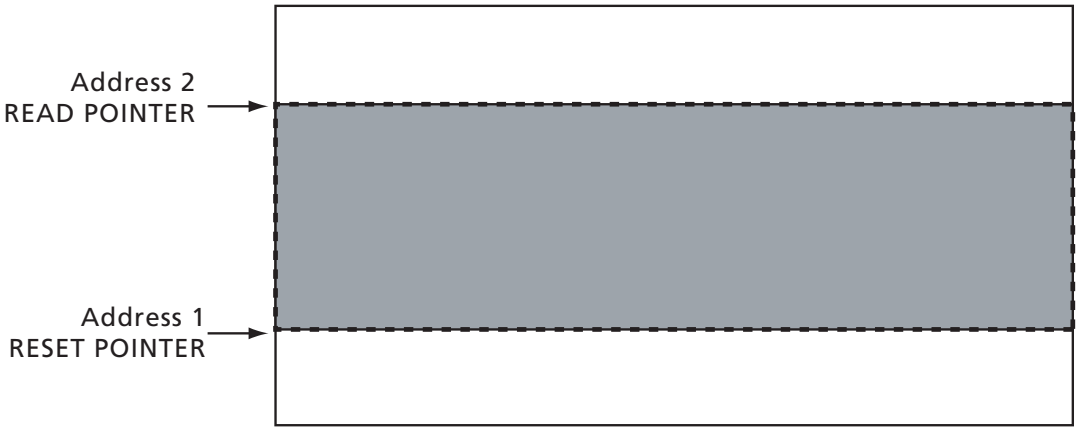
The Row Read Cycle diagram in 13 indicates the signal relationships. Address1 is the READ POINTER address. ROW_STRT_N is only used to read this row. After the pixel row in Address1 is read, a jump is made to Address 2 (RESET POINTER). The row of Address2 is then reset but not readout.

Figure 13: Row Read Cycle with ROL_RST Enabled



14 illustrates the ERS pictorially. In this example, integration time = (Address1 - Address2) * (Row Time). For example, if Row Time is ~3 msec (~50 MHz clock), and the user wants 1.5 msec integration time, set Address1 = Address2 + 500. The minimum integration time is one row time.

Figure 14: ERS Illustration



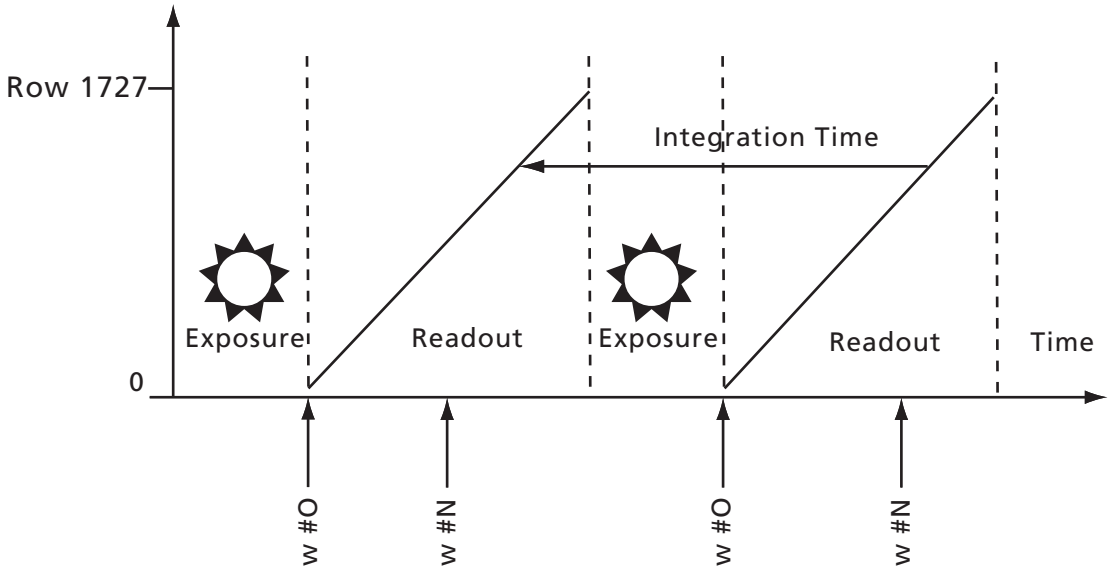
Sensor can be paused for some time and then the user decides to capture one image. Please note that the integration time for each row ends with read of the row. To provide the same integration time for all rows the following procedure is recommended:

- RESET all rows, one by one, to initiate integration. Apply ROW_STRT_N pulse every time the address is changed. Do not use LD_SHFT_N and DATA_READ_EN_N pulses.
- READ all rows to end integration and read data out. Apply ROW_STRT_N pulse to each row. After ROW_DONE_N echo, apply LD_SHFT_N and DATA_READ_EN_N pulses to read the data out and apply new ROW_STRT_N pulse.

Parallel Image Acquisition in Sensor with ERS

In typical CMOS active-pixel sensors pixels are read and reset row by row. Integration of photo- and dark-current in photo detectors starts with photodector reset. The particular row of pixels gets reset during the readout. The sequential nature of row addressing can not provide simultaneous start and end of the integration for all pixels in the array. Consequently the sensors with rolling shutters are usually referred to as sensors that are unable to “freeze the motion”. If the sensor is under dim lighting, and it is possible to use pulsed light for illuminating the scene, one can realize freeze-frame acquisition by pulsing the light between two frames as shown below. Integration still starts at different times for various rows, but integration time (duration) is the same for all rows and it includes exposure time.

Figure 15: Achieve Parallel Image



Partial Scan Examples

The MI-MV40 can be partially scanned by sub-sampling rows. The user may select which rows and how many rows to include in a partial scan. For example, with a 50-megahertz clock, a row time is approximately 2.3 microseconds, resulting in the following possibilities:

1 row in frame: ~320,000 fps
10 rows in frame: ~32,000 fps
108 rows in frame: ~3,200 fps
216 rows in frame: ~1,600 fps
432 rows in frame: ~800 fps
864 rows in frame: ~400 fps
1,728 rows in frame: ~200 fps
...etc.

Pin Descriptions

Table 3: Pin Description

PIN NUMBER(S)	SIGNAL NAME	FUNCTION
B2, G4, G3, K3,M3, N4, R4, W2, V5,W7, V10, V12, W15, W18, P15, H19,B19, E14, D14,D12, C11, E9, C7, C5	VDD_IO	Power supply for digital pad ring.
C2, E3, H4, K5, L5, M5, P4, R5, R7, T7, U8, U10, T12, R13, R15, H17, C18, A17, B14, A12, A9, B7, B5, B3	DGND_IO	Digital ground for pad ring.
	DATA [159:0]	Pixel data output bus that is sixteen pixels (160 bits) wide. Bit 0 is the LSB (least significant bit) of the lowest order pixel. In the group of sixteen pixels being output, bit 9 is the MSB (most significant bit).
T14	DATA0	
V16	DATA1	
U15	DATA2	
T15	DATA3	
U16	DATA4	
R14	DATA5	
V17	DATA6	
U17	DATA7	
T16	DATA8	
V18	DATA9	
B17	DATA10	
A19	DATA11	
A18	DATA12	
B18	DATA13	
D16	DATA14	
C17	DATA15	
E15	DATA16	
F15	DATA17	
D17	DATA18	
E16	DATA19	
V13	DATA20	
W14	DATA21	
R12	DATA22	
V14	DATA23	
U13	DATA24	
T13	DATA25	
W16	DATA26	
U14	DATA27	
V15	DATA28	
W17	DATA29	

Table 3: Pin Description (Continued)

PIN NUMBER(S)	SIGNAL NAME	FUNCTION
D13	DATA30	
E12	DATA31	
A15	DATA32	
C15	DATA33	
B15	DATA34	
A16	DATA35	
C16	DATA36	
B16	DATA37	
E13	DATA38	
D15	DATA39	
W10	DATA40	
T10	DATA41	
W11	DATA42	
V11	DATA43	
U11	DATA44	
W12	DATA45	
R11	DATA46	
T11	DATA47	
W13	DATA48	
U12	DATA49	
D11	DATA50	
B11	DATA51	
C12	DATA52	
C13	DATA53	
B12	DATA54	
E11	DATA55	
A13	DATA56	
B13	DATA57	
C14	DATA58	
A14	DATA59	
T8	DATA60	
R9	DATA61	
V8	DATA62	
U7	DATA63	
W8	DATA64	
V9	DATA65	
T9	DATA66	
W9	DATA67	
U9	DATA68	
R10	DATA69	
B8	DATA70	
A8	DATA71	
C9	DATA72	
B9	DATA73	
C10	DATA74	

Table 3: Pin Description (Continued)

PIN NUMBER(S)	SIGNAL NAME	FUNCTION
D10	DATA75	
A10	DATA76	
E10	DATA77	
B10	DATA78	
A11	DATA79	
U4	DATA80	
W4	DATA81	
T6	DATA82	
U5	DATA83	
W5	DATA84	
R8	DATA85	
V6	DATA86	
W6	DATA87	
U6	DATA88	
V7	DATA89	
A4	DATA90	
D7	DATA91	
A5	DATA92	
B6	DATA93	
E8	DATA94	
A6	DATA95	
D8	DATA96	
C8	DATA97	
A7	DATA98	
D9	DATA99	
U2	DATA100	
U3	DATA101	
T4	DATA102	
V2	DATA103	
R6	DATA104	
W1	DATA105	
V3	DATA106	
T5	DATA107	
W3	DATA108	
V4	DATA109	
E5	DATA110	
E6	DATA111	
C4	DATA112	
D5	DATA113	
A2	DATA114	
B4	DATA115	
D6	DATA116	
A3	DATA117	
E7	DATA118	
C6	DATA119	

Table 3: Pin Description (Continued)

PIN NUMBER(S)	SIGNAL NAME	FUNCTION
N3	DATA120	
R1	DATA121	
T1	DATA122	
N5	DATA123	
U1	DATA124	
T2	DATA125	
R3	DATA126	
V1	DATA127	
T3	DATA128	
P5	DATA129	
F4	DATA130	
D1	DATA131	
D3	DATA132	
C1	DATA133	
E4	DATA134	
A1	DATA135	
B1	DATA136	
F5	DATA137	
D4	DATA138	
C3	DATA139	
L2	DATA140	
L3	DATA141	
M1	DATA142	
M2	DATA143	
L4	DATA144	
N1	DATA145	
N2	DATA146	
M4	DATA147	
P1	DATA148	
P2	DATA149	
H2	DATA150	
J5	DATA151	
G1	DATA152	
G2	DATA153	
F3	DATA154	
F1	DATA155	
F2	DATA156	
H5	DATA157	
E1	DATA158	
E2	DATA159	
G5, R2, U18, D18	VDD	Power supply for core digital circuitry.
D2, P3, R16, F16	DGND	Ground for core digital circuitry.

Table 3: Pin Description (Continued)

PIN NUMBER(S)	SIGNAL NAME	FUNCTION
J2	SYSCLK	Clock input for entire chip. Maximum design frequency is 50 MHz. Clock duty cycle should be 55%±10%for operation at speeds <200fps. For operation at speeds >200 fps a clock duty cycle of 60% ±5% (i.e., clock is high 60% of the time and low 40% of the time) is recommended.
V19	DARK_OFF_EN_N	A low input enables common mode dark offset to all pixels. The value of the offset is defined by VREF3 and VCLAMP3. Subtracts a fixed offset pre-ADC. Signal is pulled up on-chip.
J3	ROW_STRT_N	Starts ADC conversion of the pixel row (defined by the row address) content. A two-clock cycle-wide active-low pulse.
L1	ROW_DONE_N	A two-cycle-wide pulse that indicates that processing of the currently addressed row has been completed.
J1	LD_SHFT_N	An active-low signal that places the recently converted row of data into output register for output, enables the sense amps and resets the column counter.
J4	DATA_READ_EN_N	An active-low signal that enables the output data multiplexer and causes the sixteen (16) 10-bit output ports to be updated with data on the rising edge of the system clock. Column counter skips data when this input is high. May always be low.
K1	CAL_STRT_N	Starts the calibration process for the ADC. This is a two-clock cycle-wide active-low pulse. This pulse must not be activated for 1ms after either power-up or removal of sensor from standby state.
K4	CAL_DONE_N	A two-clock cycle-wide active-low pulse that indicates the ADC has completed its calibration operation.
M18	VREF2	ADC reference used for the calibration operation. Adjustable external voltage from 0.4 to 1.5V is recommended. User voltage source must supply a transient current of 20 mA at a frequency of 500 kHz with a 2% duty cycle. Decoupling capacitors shown in Figure 16 on page 22 are usually sufficient to filter out this required current transient.
P17	DATA	Serial input/output of ADC calibration DAC values.
P18	DATA_CLK	Serial interface clock for ADC calibration DAC values. Recommended frequency is ~1MHz.
N16	WE_N	An active-low envelope signal that enables the writing of ADC calibration DAC values to the sensor.
P19	RE_N	An active-low envelope signal that enables the reading of A DC calibration DAC values from the sensor.
K18	VCLAMP3	Dark offset cancellation negative input reference. Adjustable external voltage from 0 to 3.0V is recommended. User voltage source must supply a transient current of 40 mA at a frequency of 500 kHz with a 2% duty cycle. Decoupling capacitors are usually sufficient to filter out this required current transient.
N15, N19, J17, G15	VREF1	ADC reference input voltage that sets them a xi mum input signal level and thus sets the size of the least significant bit (LSB) in the analog to digital conversion process. The reference value can be used like a global gain adjustment. Adjustable external voltage from 0.25 to 1.5 V is recommended. User voltage source must supply a transient current of 100 mA at a frequency of 500 kHz with a 2% duty cycle. Decoupling capacitors are usually sufficient to filter out this required current transient.

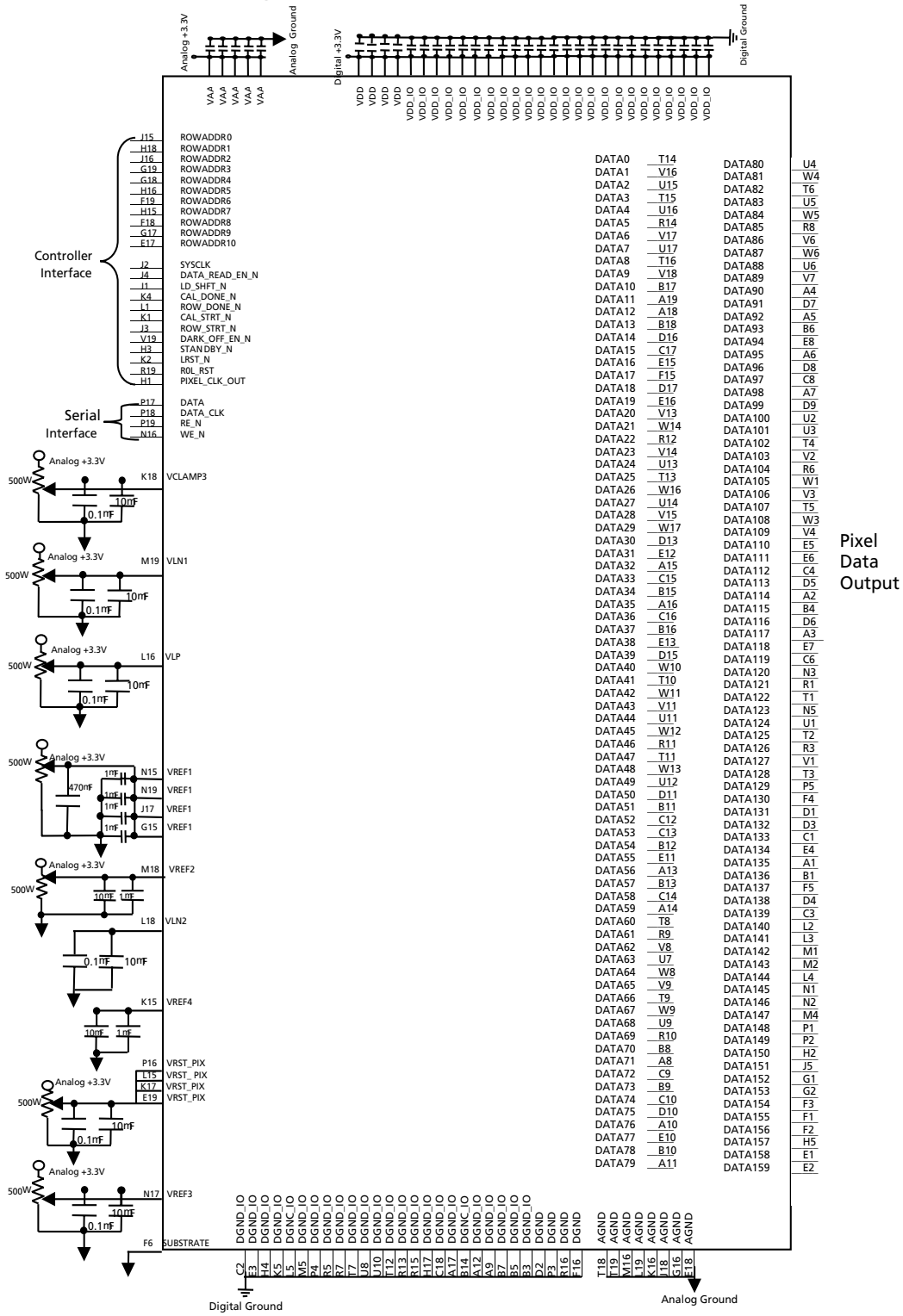
Table 3: Pin Description (Continued)

PIN NUMBER(S)	SIGNAL NAME	FUNCTION
K15	VREF4	ADC reference input. User voltage source must supply a transient current of 100 mA at a frequency of 500 kHz with a 2% duty cycle. Decoupling capacitors are usually sufficient to filter out this required current transient.
M19	VLN1	Bias setting for pixel source follower operating current. Generated on-chip. Decoupling capacitor is recommended. Range (0.5 to 1.2V) can also be adjusted externally for better performance. Impedance:10kΩ,10pF.
L18	VLN2	Bias setting voltage for ADC. Generated on-chip. Decoupling capacitor is recommended. Range (0.8 to 1.1V) can also be adjusted externally for better performance. Impedance: 10kΩ,10pF.
L16	VLP	Bias setting voltage for the column source follower operating current. Generatedon-chip. Decoupling capacitor is recommended. Range (1.0 to 2.3V) can also be adjusted externally for better performance. Impedance:10kΩ,10pF.
K2	LRST_N	Global logic reset function (asynchronous). Active-low pulse. This signal also automatically initiates an ADC calibration sequence.
H3	STANDBY_N	A low input sets the sensor in a low power mode. (Allow 1 microsecond before calibrating, after coming out of this mode). Signal is pulled up on-chip.
H1	PIXEL_CLK_OUT	Data synchronous output. User may prefer to use this pin as data clock instead of SYSCLK.
R19	ROL_RST	An active-high envelope signal that enables a faster rolling reset of the array. When unused must be grounded.
	ROW_ADDR [10:0]	10-bit bus (0 to 1723, bottom to top) that controls which pixel row is being processed or readout. An asychronous (unclocked) digital input. Must be held valid for at least 70 SYSCLK cycles. Bit 10 is the MSB.
J15	ROW_ADDR0	
H18	ROW_ADDR1	
J16	ROW_ADDR2	
G19	ROW_ADDR3	
G18	ROW_ADDR4	
H16	ROW_ADDR5	
F19	ROW_ADDR6	
H15	ROW_ADDR7	
F18	ROW_ADDR8	
G17	ROW_ADDR9	
E17	ROW_ADDR10	
T17, N18, L17, J19, F17	VAA	Power supply for analog processing circuitry (column buffers, ADC, and support).
T18, T19, M16, L19, K16, J18, G16, E18	AGND	Ground for analog signal processing circuitry.

Table 3: Pin Description (Continued)

PIN NUMBER(S)	SIGNAL NAME	FUNCTION
N17	VREF3	Dark offset cancellation positive input reference, tied to the pedastal voltage to be added to the signal. Adjustable external voltage from 0 to 3.0V is recommended. User voltage source must supply a transient current of 40 mA at a frequency of 500 kHz with a 2% duty cycle. Decoupling capacitors are usually sufficient to filter out this required current transient.
P16, L15, K17, E19	VRST_PIX	Power supply for pixel array. User voltage source must supply a transient current of 10 mA at a frequency of 500 kHz or a few amps, once a frame. Recommended range is 3.1± 0.2V. Decoupling capacitors are usually sufficient to filter out this required current transient.
F6	SUBSTRATE —	Package cavity contact. Connect to AGND. No connect.
M17, K19, D19, C19, W19, U19, R17, R18, M15		No Connect

Figure 16: Board Connections



NOTE:

1. It is recommended to use 10µ and 470µF electrolytic and 0.1µF and 1µF ceramic capacitors.
2. It is recommended that 1µF capacitors for VREF1, VREF2 and VREF4 be placed as physically close as possible to the MI-MV40 package.
3. Alternatively, the analog voltages depicted as being generated from potentiometers could be supplied from DACs.
4. The analog voltages VCLAMP3, VREF3, VLN1, VLN2, VLP, and VREF4 are generated on-chip, but user may supply voltages to override the internal biases.

Electrical Specifications

Table 4: AC Electrical Characteristics

(Vsupply = 3.3V ±0.3V)

SYMBOL	CHARACTERISTIC	CONDITION	MIN.	TYP.	MAX.	UNIT
Tplh	Data output propagation		1	2	3	ns
	delay for low to high trans.					
Tphl	Data output propagation delay		1	2	3	ns
	for high to low trans.					
Tsetup	Setup time for input to SYSCLK	Vin = Vpwr or Vgnd	3	4		ns
Thold	Hold time for input to SYSCLK	Vpwr=Min,VOH min	3	4		ns

Table 5: DC Electrical Characteristics

(Vsupply = 3.3V ±0.3V)

SYMBOL	CHARACTERISTIC	CONDITION	MIN.	TYP.	MAX.	UNIT
VDD	Digital power supply		2.9	3.3	4	V
VLP	Bias for Column Buffers		1.0	1.9	2.3	V
VREF1	Reference for ADC		0.25	1.0	1.5	V
VREF2	Reference for ADC Calibration		0.4	0.7	1.5	V
VREF3	Dark offset (positive)		0	0.15	3.0	V
VLN1	Bias for pixel source follower		0.5	1.0	1.2	V
VLN2	Bias for ADC		0.8	Open	1.1	
VRST_PIX	Pixel Array Power		2.9	3.3	3.3	V
VCLAMP3	Dark offset (negative)		0	0	3.0	V
VREF4	Reference for ADC		Open (decoupled) or 0.25* VREF1			
VIH	Input High Voltage		2.0		Vpwr+0.3	V
VIL	Input Low Voltage		-0.3		0.8	V
IIN	Input Leakage Current,					
	No Pullup Resistor	Vin = Vpwr or Vgnd	-5		5	µA
VOH	Output High Voltage	Vpwr=Min, IOH=-100µA	Vpwr-0.5			V
VOL	Output Low Voltage	Vpwr=Min, IOL=100µA			0.5	V
Ipwr	Maximum Supply Current	50 MHz clock, 5pF load on outputs		200		mA

Table 6: DC Absolute Maximum Ratings[1]

SYMBOL	PARAMETER	VALUE	UNIT
Vpwr	DC Supply Voltage	-0.5 to 3.6	V
Vin	DC Input Voltage	-0.5 to Vpwr + 0.5	V
Vout	DC Output Voltage	-0.5 to Vpwr + 0.5	V
I	DC Current Drain per Pin (Any I/O)	±50	mA
I	DC Current Drain, Vpwr and Vgnd	±100	mA

NOTE:

1. Maximum Ratings are those values beyond which damage to the device may occur.
   Vpwr=VDD=VAA=VDD_IO (VDD is supply to digital circuit, VAA to analog circuit).
   Vgnd=DGND=AGND (DGND is the ground to the digital circuit, AGND to the analog circuit).

Table 7: Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX[1]	UNIT
Vpower	DC Supply Voltage	3.00	3.6	V
T_A	Commercial Operating Temperature	-5	60	°C
T_J	Junction Temperature	0	85	°C

NOTE:

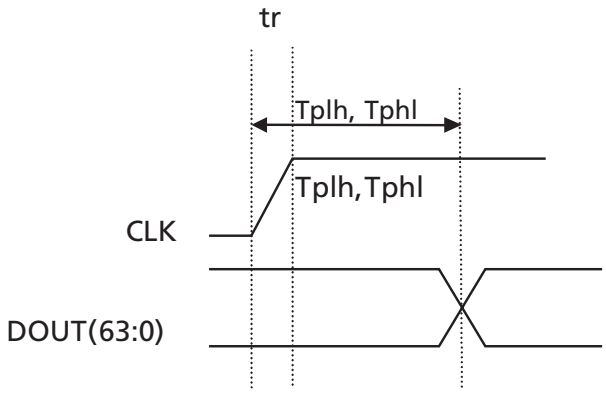
1. This device contains circuitry to protect the inputs against damage from high static voltages or electric fields, but the user is advised to take precautions to avoid the application of any voltage higher than the maximum rated.

Table 8: Power Dissipation

(Vpwr = 3.3V; T_A= 25 °C; 200 fps)

SYMBOL	PARAMETER	TYPICAL	UNIT
Pavg	Average Power	≤700	mW

Figure 17: Clock to Data Propagation Delay



Optical Specifications

Table 9: Image Sensor Characteristics

(T_A= 25 °C)

SYMBOL	PARAMETER	TYP	UNIT
R_I	Responsivity (ADC VREF1=1V)	2,500	LSB/lux-sec.
PRNU	Photo response non-uniformity	1	%rms
Nsat	Pixel saturation level	25,000	electrons
Vdrk	Output referred dark signal	40	mV/sec
NE	Input referred noise: Overlapped conversion and digital readout (200 fps)	30	electrons
Dyn_I	Internal dynamic range	60	dB
DSNU	Dark signal non-uniformity	0.1	%rms
CG	Conversion gain	30	µV/e^-
Kdrk	Dark current temperature coefficient	100	%/8°C

Table 10: Pixel Array

SYMBOL	PARAMETER	TYP	UNIT
Resolution	Number of pixels in active image	2352 x 1728	pixels
Pixel size	X-Y dimensions	7 x 7	µm
Pixel pitch	Center-to-center pixel spacing	7	µm
Pixel fill factor	Area of drawn active area	55	%

Lens Selection

Much of the specific information in this section is explained in detail in the Technology section on the website. The following information applies specifically to the MI-MV40 megapixel image sensor.

Format

The diagonal of the image sensor array 20.43mm, fits most closely, but not exactly, within the optical format corresponding to the 1-inch specification. Some 1-inch optical format lenses have been shown to work well with this sensor. Typical 1-inch lens examples are Computer V2513, V5013, and V7514. F-mount lenses provide another possible lens solutionduetotheirlarge-imagecircle.

Mounting

Several lens mounting standards exist that specify the threading of the lens' barrel as well as the distance the back flange of the lens should be from the image sensor for the lens to properly form an image. Typical lens mounting standards for the MI-MV40 are:

Table 11: Mounting Types

MOUNT NAME	MOUNTING THREADS	BACK-FLANGE-TO-IMAGE-SENSOR
C	1 - 32	17.526 mm
CS	1 - 32	12.5 mm

Another option is to use a C-mount together with a C-to F-mount adapter for greater lens flexibility.

Field of View and Focal Length

The field of view of an imaging system will depend on both the focal length of the imaging lens and the width of the image sensor. As most of the image information humans pay attention to generally falls within a 45-degree horizontal field of view, many camera systems attempt to imitate this field of view. However, in some cases a telephoto system (with a narrow field of view, say less than 20 degrees), or a wide angle system (with a wide field of view, say more than 60 degrees) may be desired. The approximate field of view that an imaging system can achieve is shown in the following equation:

$$\theta \approx 2\tan^{-1}\left(\frac{w}{2f}\right)$$

where θ is the field of view, $\tan^{-1}$ is the trigonometric function arc-tangent, w is the width of the image sensor, and f is the focal length of the imaging lens. For example, the imaging system's diagonal field of view can be determined by using the diagonal of the image sensor (19.67mm) for w and a particular lens' focal length for f. Alternatively, the imaging system's horizontal field of view can be determined by using the horizontal of the image sensor (15.36 mm) for w and a particular lens' focal length for f. A lens with an approximately 50mm focal length will provide an 18-degree horizontal field of view with a MI-MV40 (keep in mind that the above equation is a simplified approximation).

F-Number

The f-number, or f-stop, of an imaging lens is the ratio of the lens' focal length to its open aperture diameter. Every doubling in f-number reduces the light to the sensor by a factor of four. For example, a lens set at f/1.4 lets in four times more light than that same lens when it is set at f/2.8. Low f-number lenses capture a lot of light for delivery to the image sensor, but also require careful focus. Higher f-number lenses capture less light for delivery to the image sensor, and do not require as much effort to bring the imaging system to focus. Low f-number lenses generally cost more than high f-number lenses of similar overall performance. Typical f-numbers for various imaging systems are:

Table 12: Typical F-Numbers

F/#	IMAGING APPLICATION
1.4	Low-light level imaging, manual focus systems
2.0	Typical for PC and other small form cameras
2.8	Common in digital still cameras
4.0+	Often used in machine vision applications

MTF

Modulation Transfer Function (MTF) is a technical term that quantifies how well a particular system propagates information. For cameras, the "system" is the lens and the sensor, and the "information" is the picture they are capturing. MTF ranges from zero (no information gets through) to 100 (all information gets through), and is always specified in terms of information density. In most imaging systems, the MTF is limited by the performance of the imaging lens. A lens must be able to transfer enough information to the image sensor to be able to resolve details in the image that are as small as the pixels in the image sensor. The pixels are set on a 12-micron pitch (the center of one

pixel is 12 microns from the center of its neighboring pixel). Thus, a lens used should be able to resolve image features as small as 12 microns. Typically, a lens' MTF is plotted as a function of the number of line pairs per millimeter the lens is attempting to resolve (more line pairs per millimeter mean higher information densities). For an electronic imaging system, one line pair will correspond to two image sensor pixels (each pixel can resolve one line). This is equated as:

$$\frac{LP}{mm} = \frac{1}{2z}$$

where LP/mm means line pairs per millimeter and z is the image sensor's pixel pitch, in millimeters. For the MI-MV40, z = 0.012mm, such that the MI-MV40 has 42 LP/mm. Thus, a lens should provide an acceptable level of MTF all the way out to 42 LP/mm. For most lenses, the MTF will be highest in the center of the images they form, and gradually drop off toward the edges of the images they form. As well, MTFs at low values of LP/mm will generally be larger than MTFs at high values of LP/mm. One of the many trade-offs that must be decided by the end user is how high the MTF needs to be for a particular imaging situation. Generally, near an image sensor's LP/mm good MTFs are higher than 40, moderate MTFs are from 20 to 40, and poor MTFs are less than 20.

Infrared Cut-Off Filters

In most visible imaging situations it is necessary to include a filter in the imaging path that blocks infrared (IR) light from reaching the image sensor. This filter is called an IR cut-off filter. Various forms of IR cut-off filters are available, some absorptive (like Hoya's CM500 or Schott's BG18) and some reflective (i.e., dielectric stacks). Infrared light poses a problem to visible imaging because its presence blurs and decreases the MTF in the images formed by a lens. Since human vision only extends across a narrow range of the electromagnetic spectrum, camera systems hoping to capture images that look like the images our eyes capture must not capture light outside of our vision range. Silicon-based light detectors (like the ones in the MI-MV40's pixels) detect light from the very deep blue to the near infrared. Thus, a filter must exist in the light's path that keeps the infrared from reaching the image sensor's pixels. In most cases, it is important that such a filter begin blocking light around 650 nm (in the deep red) and continue blocking it until at least 1100 nm (in the near IR). In most camera systems, the IR cut-off filter is included in the imaging lens.However, this point must be verified by a lens vendor when a particular lens is chosen for use with an image sensor.

Figure 18: Quantum Efficiency

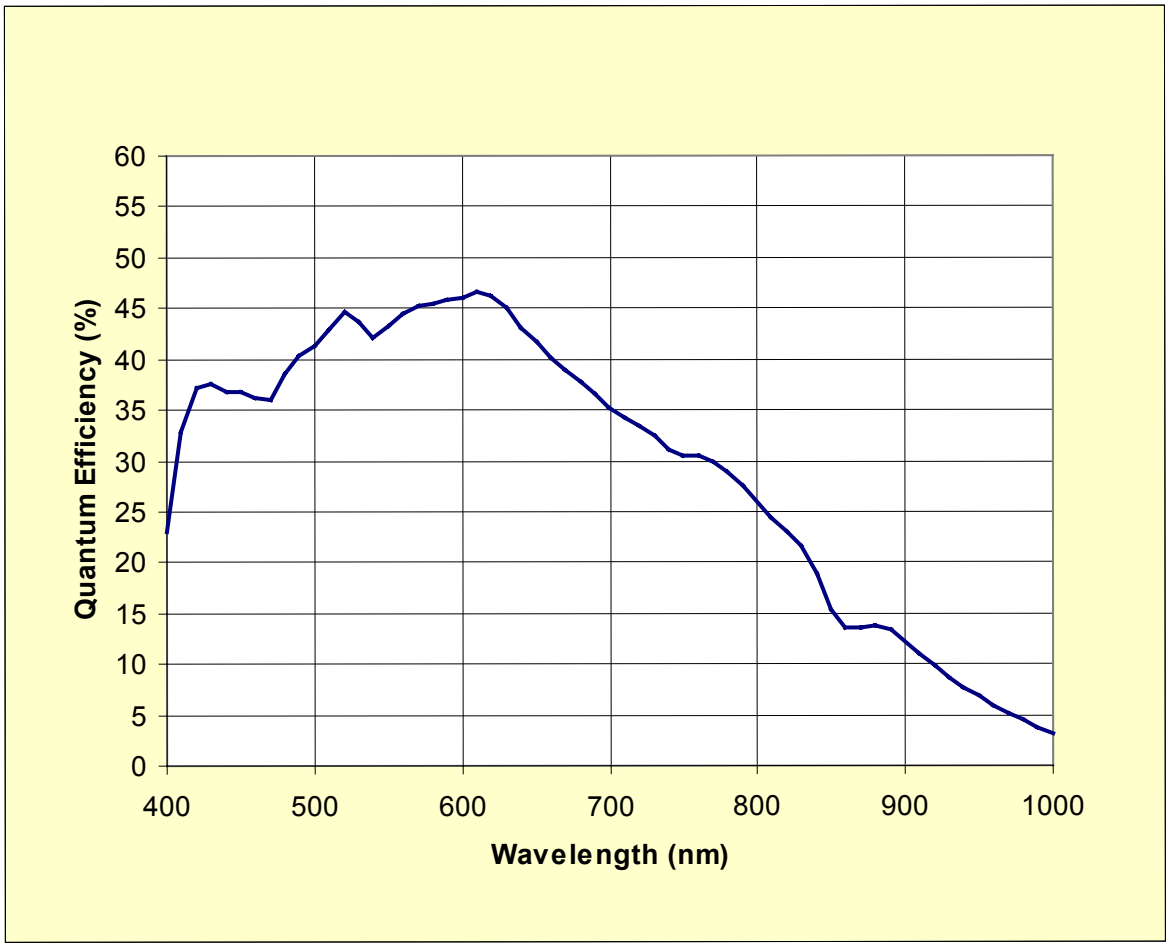
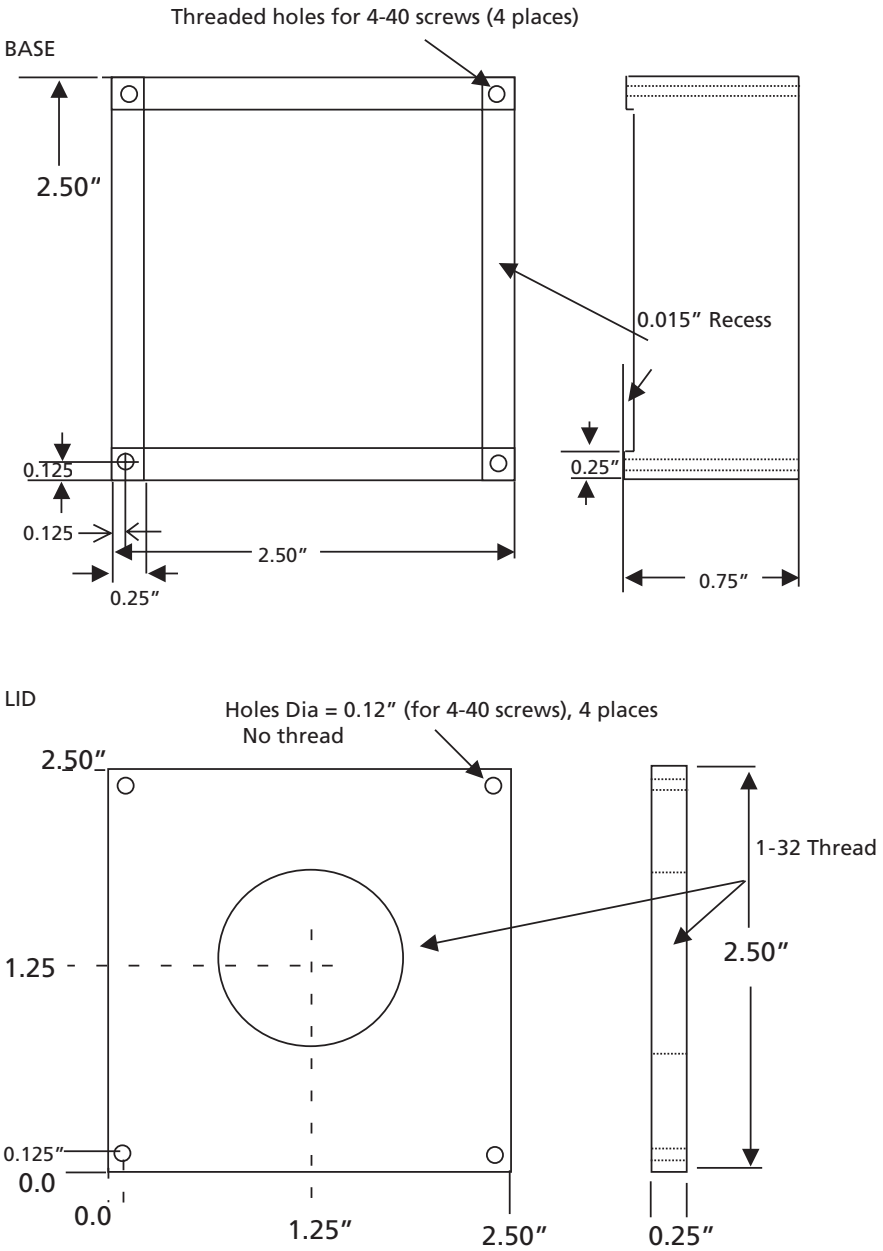


Figure 19: Quantum Efficiency - 4-Color

TBD

Figure 20: C-Mount Lens Shroud for MI-MV40 and Socket



NOTE: This shroud is designed to accommodate the MI-MV40 when it is inserted into a PGA socket. These dimensions are based on the MILL MAX #510-93-281-19-081003 socket (www.mill-max.com).

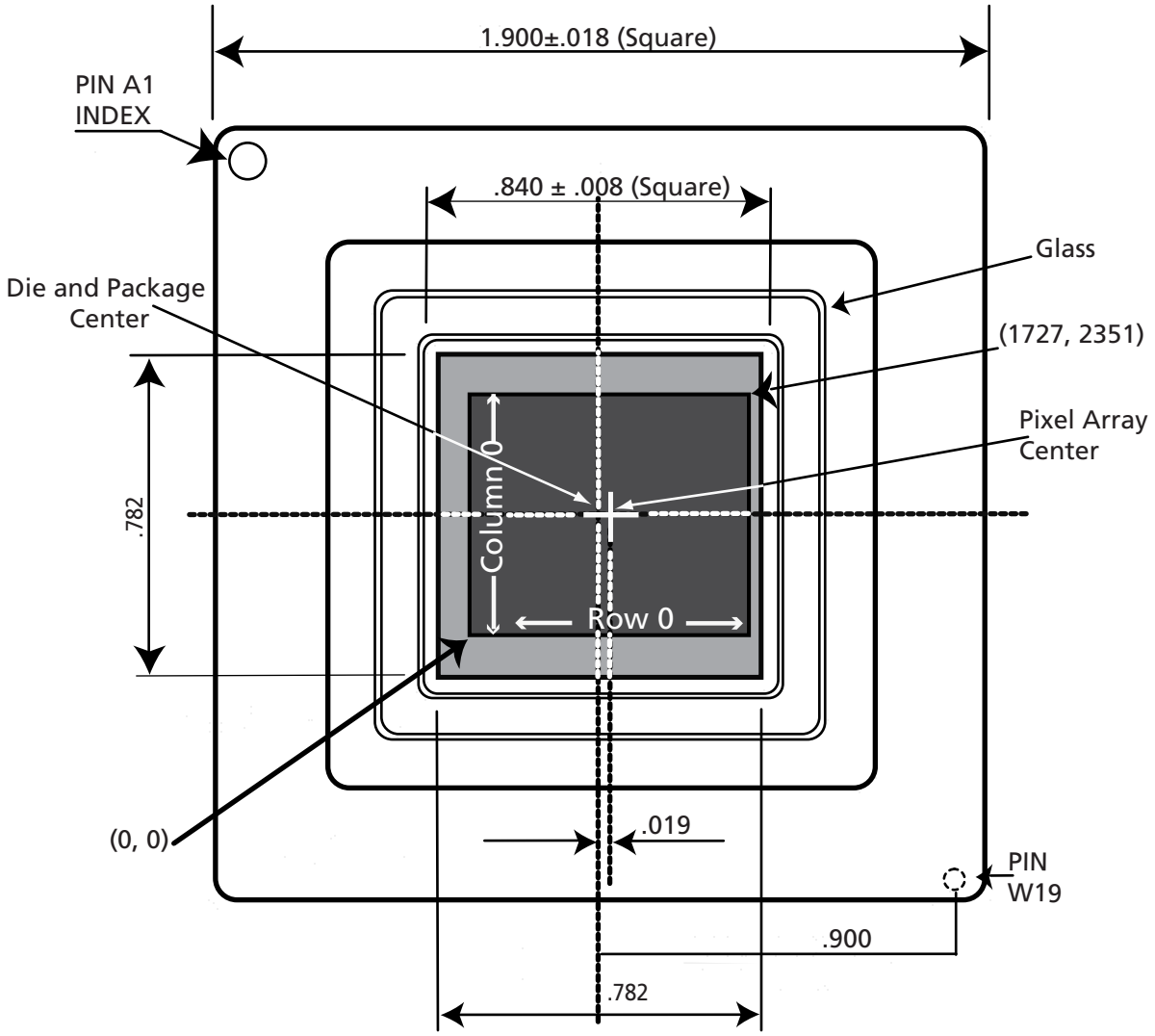
Package (280-Pin Ceramic PGA)

The MI-MV40 CMOS image sensor has a window-filled package. During manufacture the die is placed into the 280-pin ceramic PGA (pin grid array), filled with a low-viscosity epoxy, covered with a window of appropriate thickness (for the focal length), and cured. This results in a physically robust module for board installation.

Table 13: Environmental Absolute Maximum Ratings

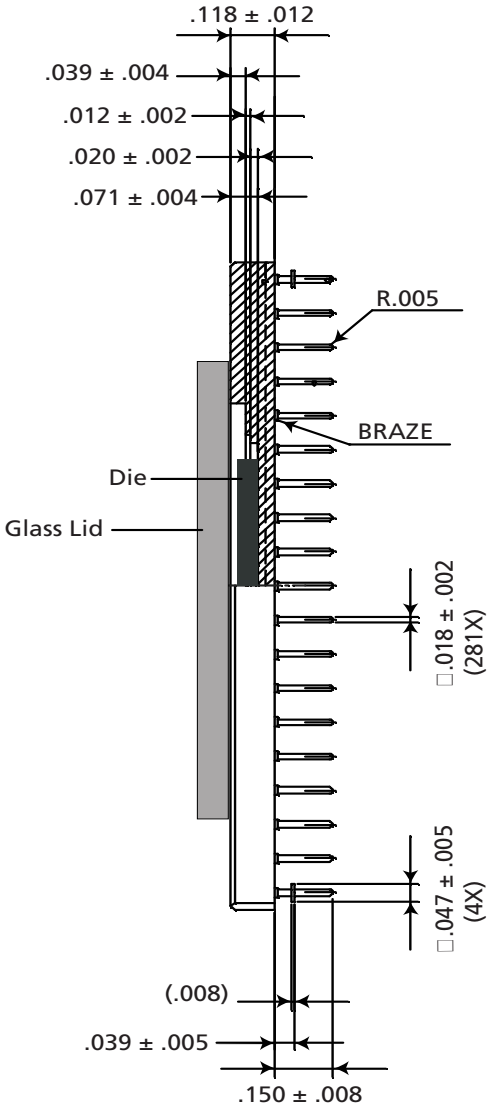
SYMBOL	PARAMETER	VALUE	UNIT
Tstorage	Storage Temperature Range	-40 to 125	°C
Tlead	Lead Temperature (10 second soldering)	235 Max.	°C

Figure 21: 280-Pin Ceramic PGA Package Top View



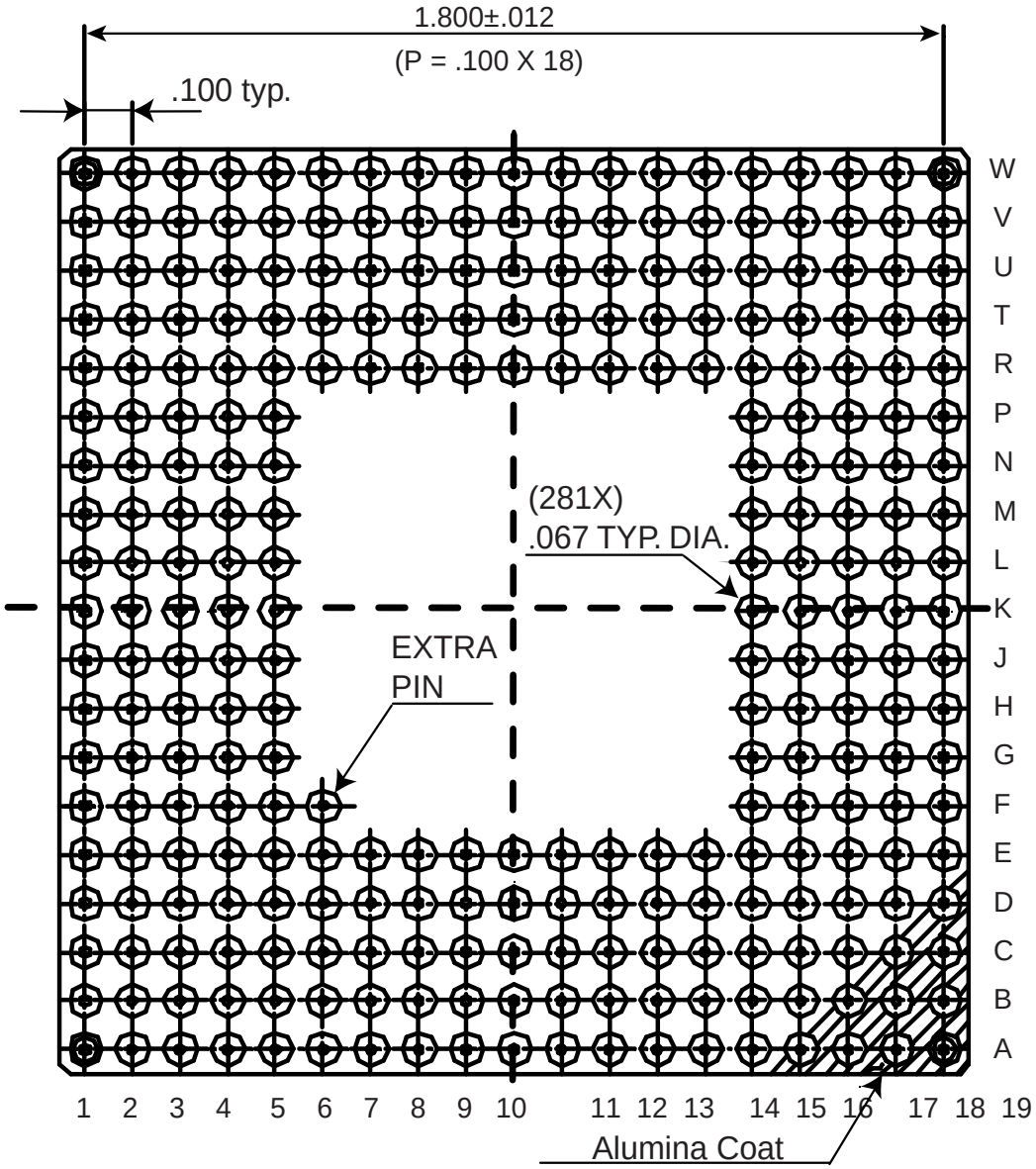
UNITS: INCHES
Note: 1. Sensor is centered on package, pixel array is off-center.
2. Die placement tolerance is ± 0.012 inches.

Figure 22: 280-Pin Ceramic PGA Package Side View



Notes:
Units: Inches
2. Die thickness .0285 ± .001.
3. Die epoxy thickness .001 ± .002.
4. D-263 glass lid thickness .031 ± .002.
5. Glass lid epoxy thickness .001 ± .002.

Figure 23: 280-Pin Ceramic PGA Package Bottom View



Data Sheet Designation

Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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