National Semiconductor

July 2001

DS90CR287/DS90CR288A +3.3V Rising Edge Data Strobe LVDS 28-Bit Channel Link-85 MHZ

General Description

The DS90CR287 transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR288A receiver converts the four LVDS data streams back into 28 bits of LVCMOS/LVTTL data. At a transmit clock frequency of 85 MHZ, 28 bits of TTL data are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHZ clock, the data throughput is 2.38 Gbit/s (297.5 Mbytes/sec). Both devices are also offered in 64 ball, 0.8mm fine pitch ball grid array (FBGA) package which provides a 44 % reduction in PCB footprint over the 56L TSSOP package.

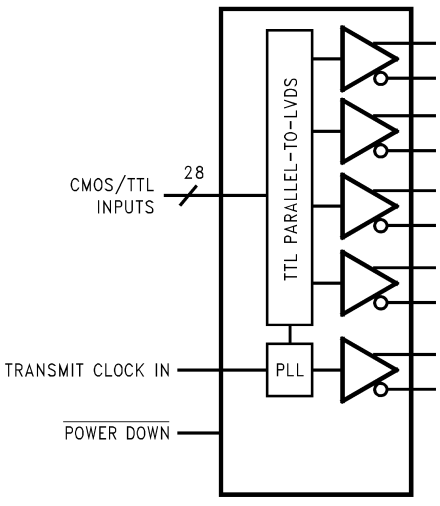
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Features

- 20 to 85 MHZ shift clock support
- 50% duty cycle on receiver output clock
- 2.5 / 0 ns Set & Hold Times on TxINPUTs
- Low power consumption
- ±1V common mode range (around +1.2V)
- Narrow bus reduces cable size and cost
- Up to 2.38 Gbps throughput
- Up to 297.5 Megabytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead TSSOP package
- Both devices are also available in 64 ball, 0.8mm fine pitch ball grid array (FBGA) package

Block Diagrams

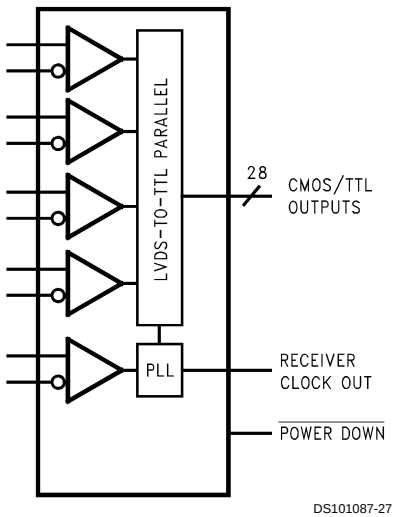
DS90CR287



DS101087-1

Order Number DS90CR287MTD or DS90CR287SLC
See NS Package Number MTD56 or SLC64A

DS90CR288A



DS101087-27

Order Number DS90CR288AMTD or DS90CR288ASLC
See NS Package Number MTD56 or SLC64A

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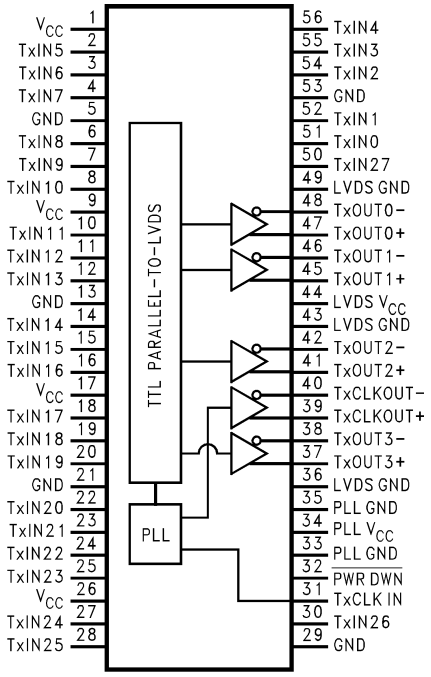
Pin Diagram for TSSOP Packages

DS90CR287



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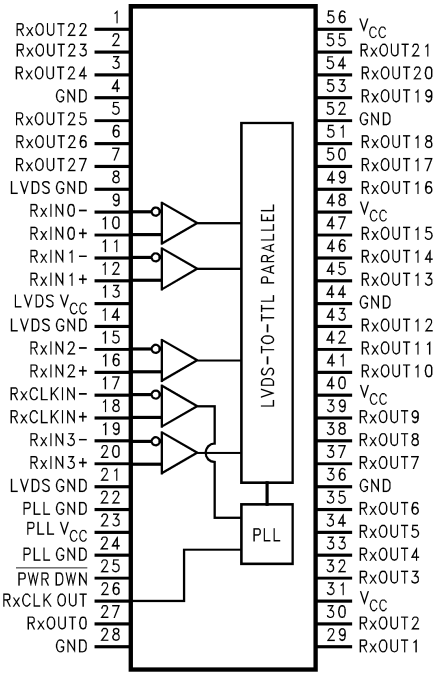
DS90CR288A



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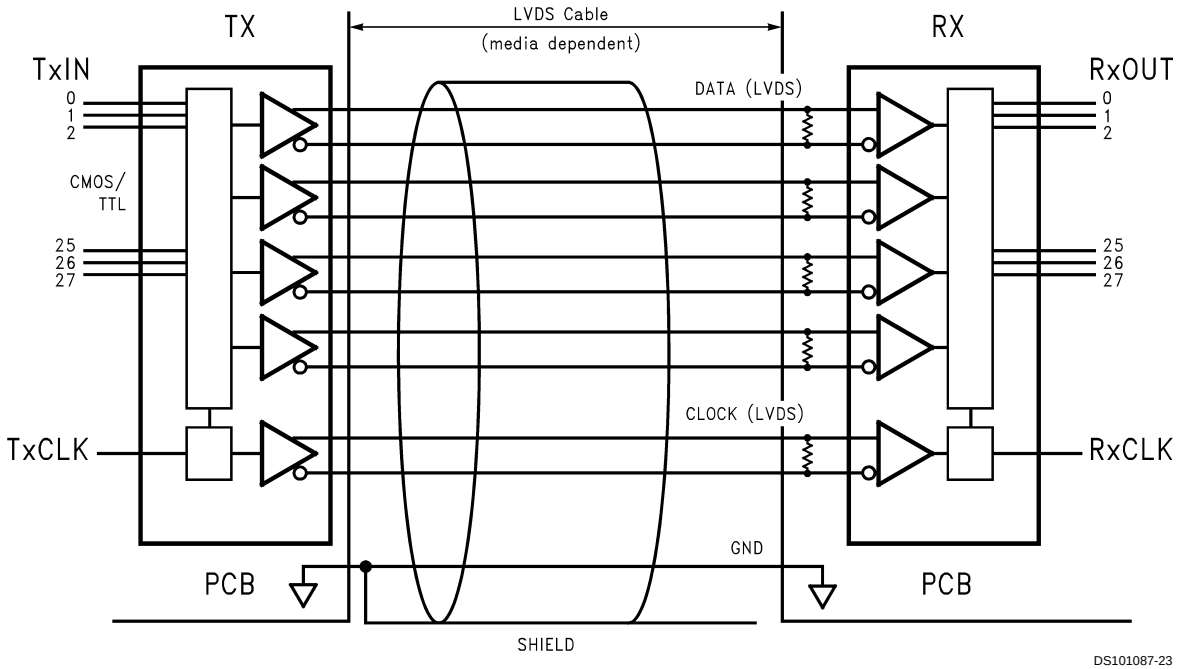
Typical Application



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.5V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec.)	+260˚C
Solder Reflow Temperature (20 sec for FBGA)	+220˚C
Maximum Package Power Dissipation @ +25˚C	
MTD56 (TSSOP) Package:	
DS90CR287MTD	1.63 W
DS90CR288AMTD	1.61 W
Package Derating:	
DS90CR287MTD	12.5 mW/˚C above +25˚C
DS90CR288AMTD	12.4 mW/˚C above +25˚C
Maximum Package Power Dissipation @ +25˚C	
SLC64A Package:	
DS90CR287SLC	2.0 W
DS90CR288ASLC	2.0 W
Package Derating:	
DS90CR287SLC	10.2 mW/˚C above +25˚C
DS90CR288ASLC	10.2 mW/˚C above +25˚C
ESD Rating	
(HBM, 1.5kΩ, 100pF)	> 7kV
(EIAJ, 0Ω, 200pF)	> 700V
Latch Up Tolerance @ +25˚C	> ±300mA

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{PP}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA	2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.06	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}		+1.8	+15	µA
		V_{IN} = GND	−10	0		µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		−60	−120	mA
LVDS DRIVER DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OS}	Offset Voltage (Note 4)		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω		−3.5	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{PWR\ DWN}$ = 0V, V_{OUT} = 0V or V_{CC}		±1	±10	µA
LVDS RECEIVER DC SPECIFICATIONS						
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V			+100	mV
V_{TL}	Differential Input Low Threshold		−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V			±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V			±10	µA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current Worst Case (with Loads)	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (*Figures 1, 2*)	f = 33 MHz		31	45	mA
			f = 40 MHz		32	50	mA
			f = 66 MHz		37	55	mA
			f = 85 MHz		42	60	mA
I_{CCTZ}	Transmitter Supply Current Power Down	$\overline{PWR\ DWN}$ = Low Driver Outputs in TRI-STATE under Powerdown Mode			10	55	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern (*Figures 1, 3*)	f = 33 MHz		49	70	mA
			f = 40 MHz		53	75	mA
			f = 66 MHz		81	114	mA
			f = 85 MHz		96	135	mA
I_{CCRZ}	Receiver Supply Current Power Down	$\overline{PWR\ DWN}$ = Low Receiver Outputs Stay Low during Powerdown Mode			140	400	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25˚C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: V_{OS} previously referred as V_{CM}.

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (*Figure 2*)			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time (*Figure 2*)			0.75	1.5	ns
TCIT	TxCLK IN Transition Time (*Figure 4*)		1.0		6.0	ns
TPPos0	Transmitter Output Pulse Position for Bit0 (*Figure 14*)	f = 85 MHz	−0.20	0	0.20	ns
TPPos1	Transmitter Output Pulse Position for Bit1		1.48	1.68	1.88	ns
TPPos2	Transmitter Output Pulse Position for Bit2		3.16	3.36	3.56	ns
TPPos3	Transmitter Output Pulse Position for Bit3		4.84	5.04	5.24	ns
TPPos4	Transmitter Output Pulse Position for Bit4		6.52	6.72	6.92	ns
TPPos5	Transmitter Output Pulse Position for Bit5		8.20	8.40	8.60	ns
TPPos6	Transmitter Output Pulse Position for Bit6		9.88	10.08	10.28	ns
TCIP	TxCLK IN Period *(Figure 5)*		11.76	T	50	ns
TCIH	TxCLK IN High Time (*Figure 5*)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time (*Figure 5*)		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN (*Figure 5*)	f = 85 MHz	2.5			ns
THTC	TxIN Hold to TxCLK IN (*Figure 5*)		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay (*Figure 7*)	T_A = 25˚C, V_{CC} = 3.3V	3.8		6.3	ns
TPLLS	Transmitter Phase Lock Loop Set (*Figure 9*)				10	ms
TPDD	Transmitter Powerdown Delay (*Figure 12*)				100	ns
TJIT	TxCLK IN Cycle-to-Cycle Jitter (Input clock requirement)				2	ns

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (*Figure 3*)			2	3.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time (*Figure 3*)			1.8	3.5	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (*Figure 15*)	f = 85 MHz	0.49	0.84	1.19	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.17	2.52	2.87	ns
RSPos2	Receiver Input Strobe Position for Bit 2		3.85	4.20	4.55	ns
RSPos3	Receiver Input Strobe Position for Bit 3		5.53	5.88	6.23	ns
RSPos4	Receiver Input Strobe Position for Bit 4		7.21	7.56	7.91	ns
RSPos5	Receiver Input Strobe Position for Bit 5		8.89	9.24	9.59	ns
RSPos6	Receiver Input Strobe Position for Bit 6		10.57	10.92	11.27	ns
RSKM	RxIN Skew Margin (Note 5) (*Figure 16*)	f = 85 MHz	290			ps
RCOP	RxCLK OUT Period (*Figure 6*)		11.76	T	50	ns
RCOH	RxCLK OUT High Time (*Figure 6*)	f = 85 MHz	4	5	6.5	ns
RCOL	RxCLK OUT Low Time (*Figure 6*)		3.5	5	6	ns
RSRC	RxOUT Setup to RxCLK OUT (*Figure 6*)		3.5			ns
RHRC	RxOUT Hold to RxCLK OUT (*Figure 6*)		3.5			ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25˚C, V_{CC} = 3.3V (Note 6)(*Figure 8*)		5.5	7	9.5	ns
RPLLS	Receiver Phase Lock Loop Set (*Figure 10*)				10	ms
RPDD	Receiver Powerdown Delay (*Figure 13*)				1	µs

Note 5: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window-RSPOS). This margin allows LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and source clock (less than 150 ps).

Note 6: Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for the 217/287 transmitter and 218/288A receiver is: (T + TCCD) + (2*T + RCCD), where T = Clock period.

AC Timing Diagrams

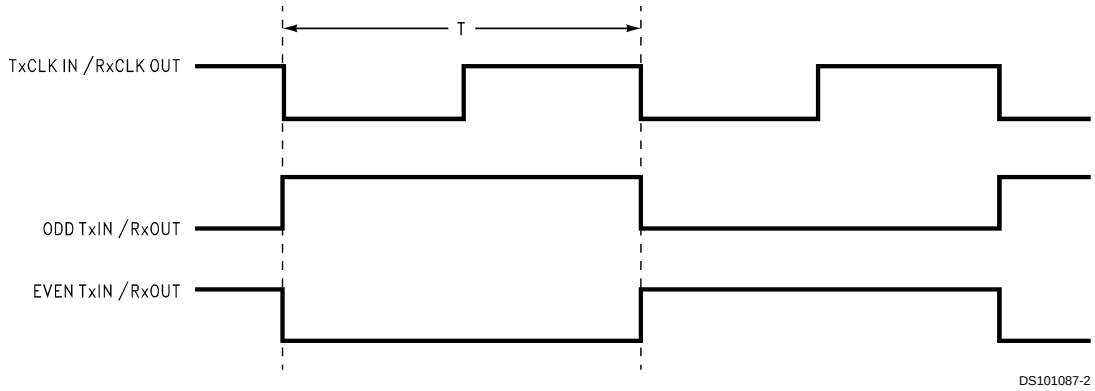

FIGURE 1. "Worst Case" Test Pattern

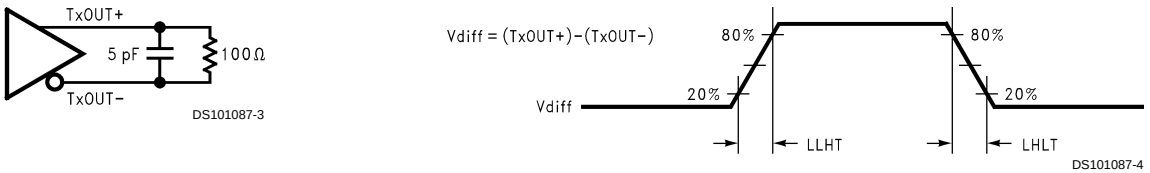

FIGURE 2. DS90CR287 (Transmitter) LVDS Output Load and Transition Times

AC Timing Diagrams (Continued)

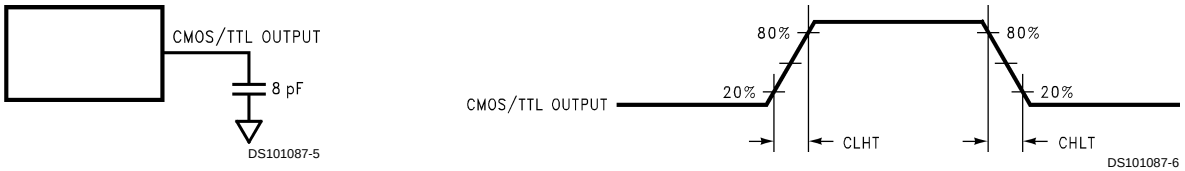

FIGURE 3. DS90CR288A (Receiver) CMOS/TTL Output Load and Transition Times

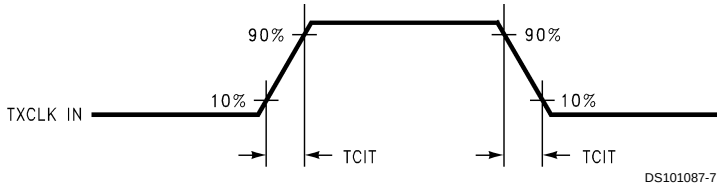

FIGURE 4. DS90CR287 (Transmitter) Input Clock Transition Time

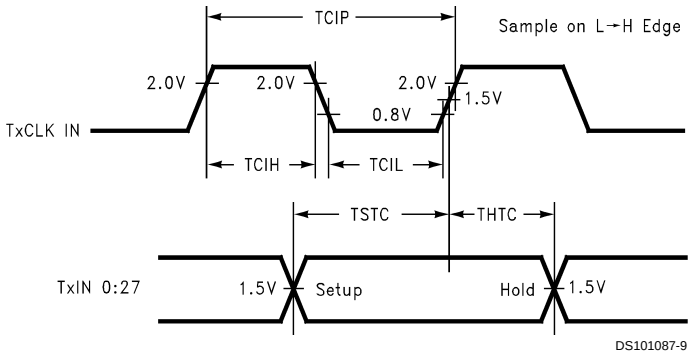

FIGURE 5. DS90CR287 (Transmitter) Setup/Hold and High/Low Times

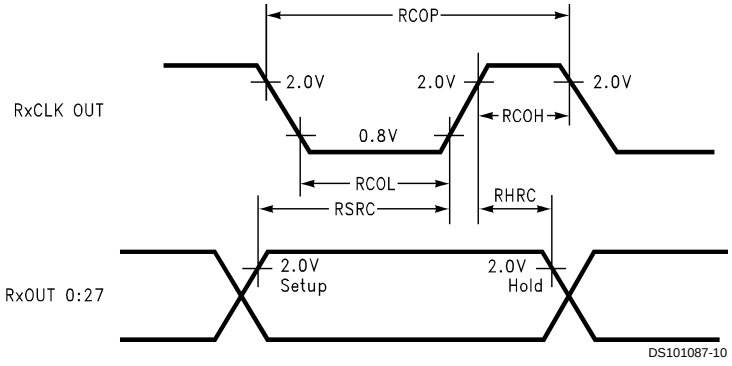

FIGURE 6. DS90CR288A (Receiver) Setup/Hold and High/Low Times

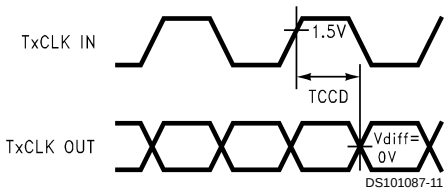

FIGURE 7. DS90CR287 (Transmitter) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

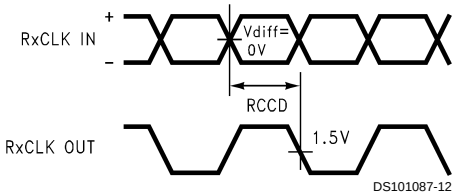

FIGURE 8. DS90CR288A (Receiver) Clock In to Clock Out Delay

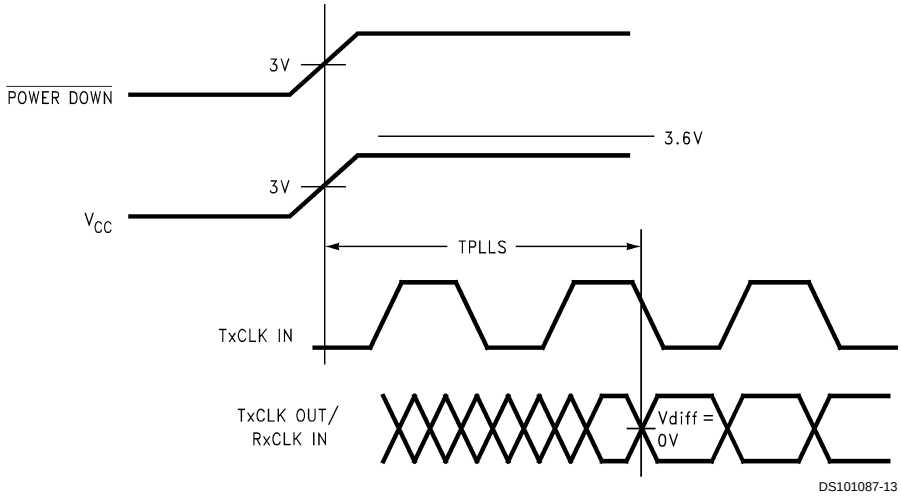

FIGURE 9. DS90CR287 (Transmitter) Phase Lock Loop Set Time

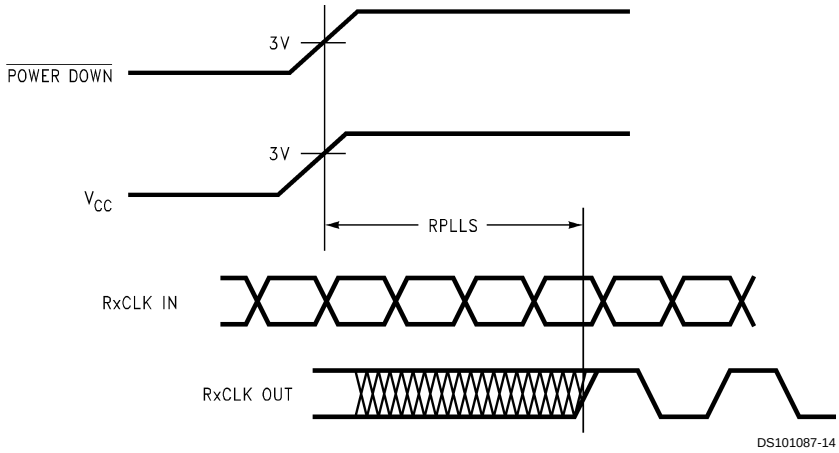

FIGURE 10. DS90CR288A (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

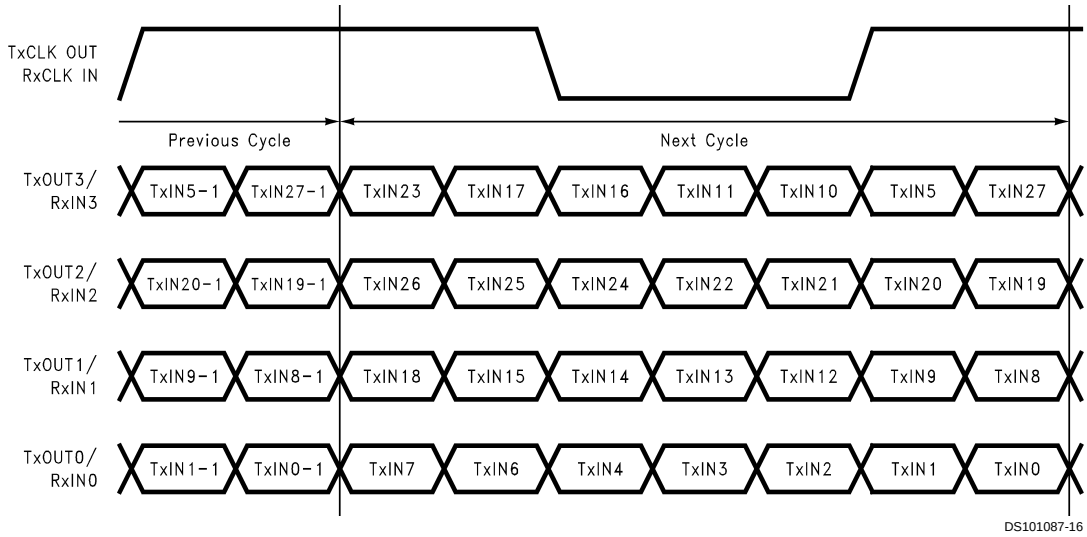

FIGURE 11. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs

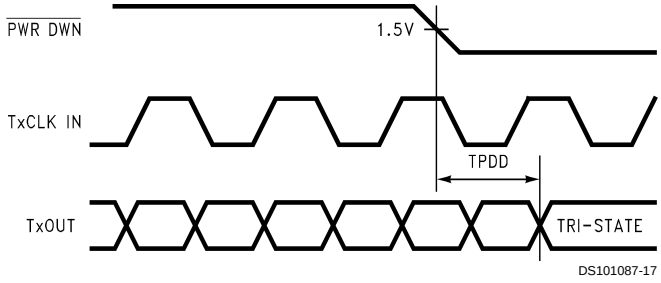

FIGURE 12. Transmitter Powerdown Delay

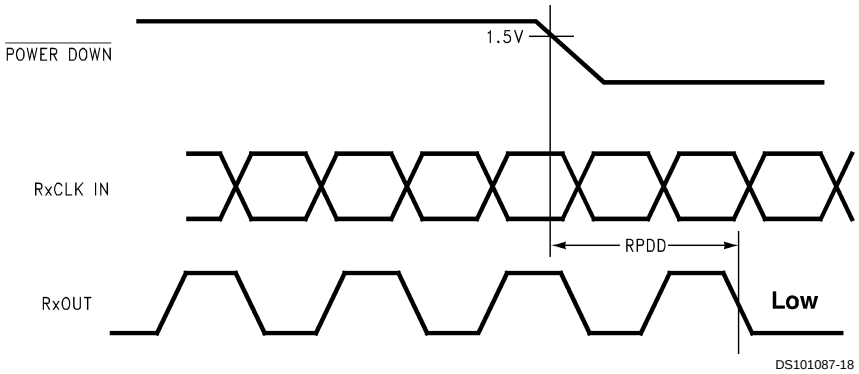

FIGURE 13. Receiver Powerdown Delay

AC Timing Diagrams (Continued)

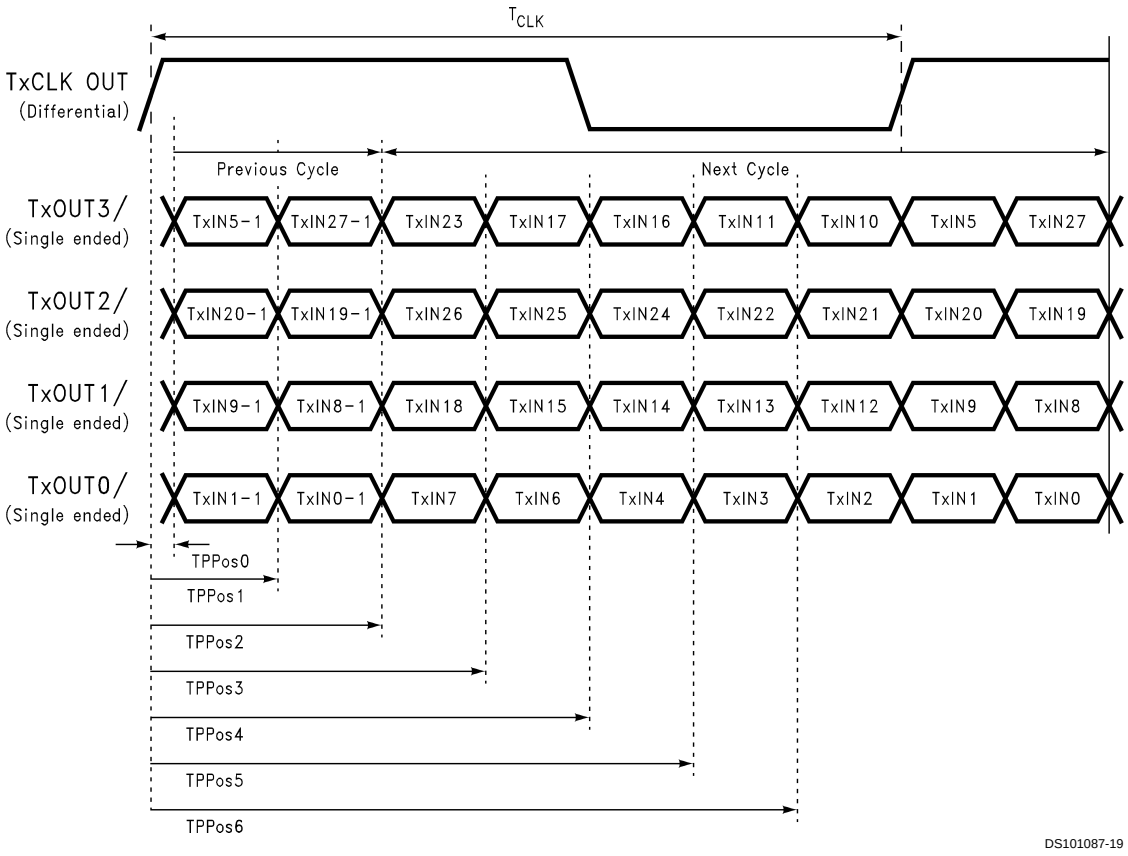

FIGURE 14. Transmitter LVDS Output Pulse Position Measurement

Applications Information (Continued)

ramic type in surface mount form factor) between each V_{CC} and the ground plane(s) are recommended. The three capacitor values are 0.1 µF, 0.01µF and 0.001 µF. An example is shown in *Figure 18*. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL V_{CC} should receive the most filtering/bypassing. Next would be the LVDS V_{CC} pins and finally the logic V_{CC} pins.

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FIGURE 17. LVDS Serialized Link Termination

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FIGURE 18. CHANNEL LINK Decoupling Configuration

CLOCK JITTER: The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 85 MHZ clock has a period of 11.76 ns which results in a data bit width of 1.68 ns. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

INPUT CLOCK: The input clock should be present at all times when the part in enabled. If the clock is stopped, the $\overline{\text{PWR DOWN}}$ pin should be asserted to disable the PLL. Once the clock is active again, the part can then be enabled. Do not enable the part without a clock present.

COMMON MODE vs. DIFFERENTIAL MODE NOISE MARGIN: The typical signal swing for LVDS is 300 mV centered at +1.2V. The CHANNEL LINK receiver supports a 100 mV threshold therefore providing approximately 200 mV of differential noise margin. Common mode protection is of more importance to the system's operation due to the differential data transmission. LVDS supports an input voltage range of Ground to +2.4V. This allows for a ±1.0V shifting of the center point due to ground potential differences and common mode noise.

POWER SEQUENCING AND POWERDOWN MODE: Outputs of the CNANNEL LINK transmitter remain in TRI-STATE® until the power supply reaches 2V. Clock and data outputs will begin to toggle 10 ms after V_{CC} has reached 3V and the Powerdown pin is above 1.5V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to 5 µW (typical).

The CHANNEL LINK chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to V_{CC} through an internal diode. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.

Applications Information (Continued)

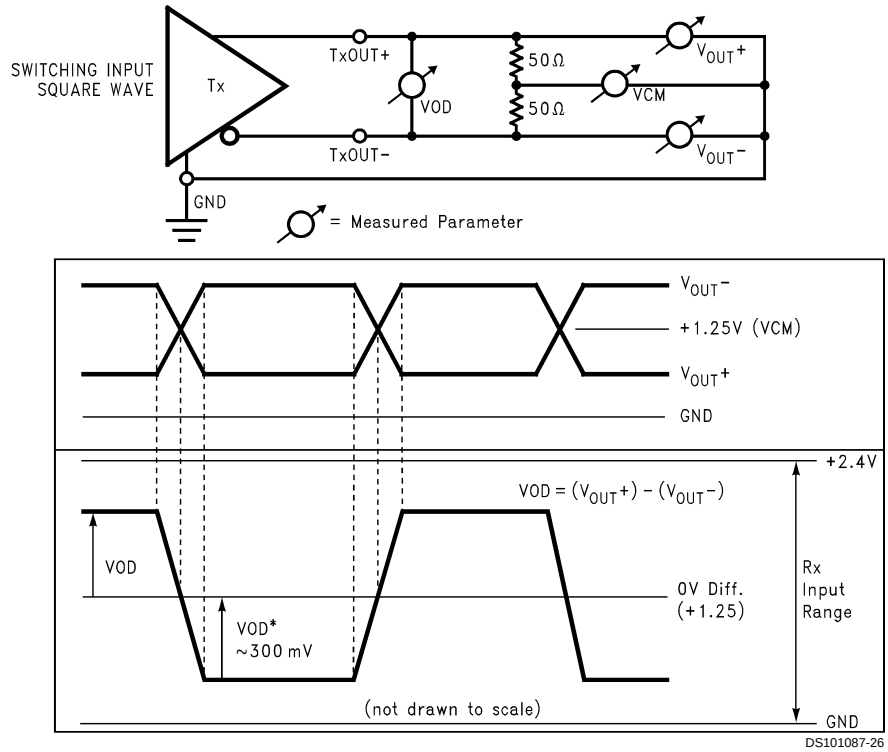
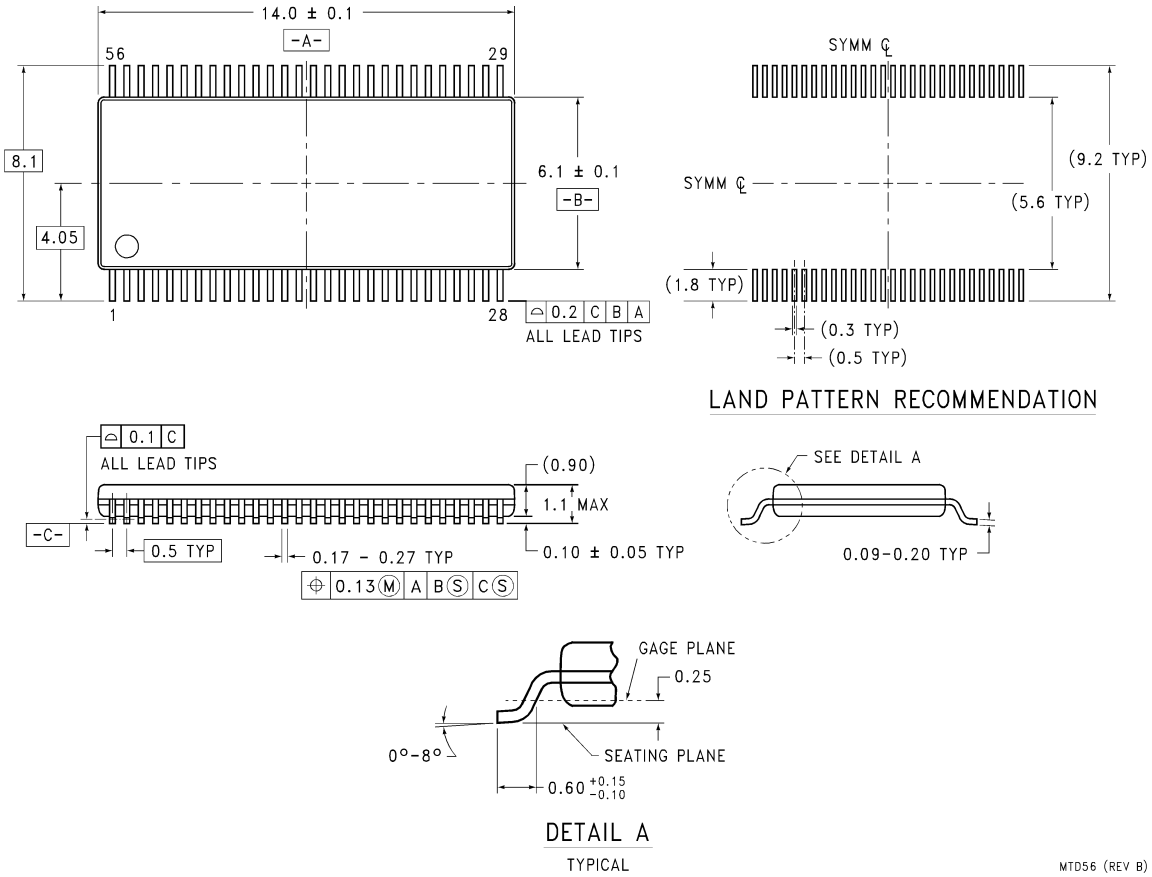
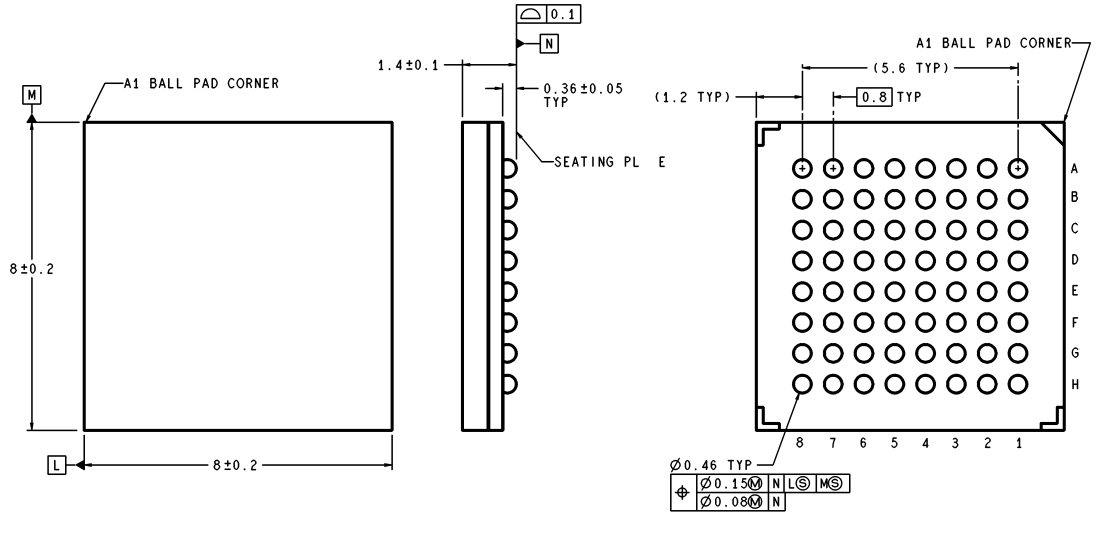


FIGURE 19. Single-Ended and Differential Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Molded Thin Shrink Small outline Package, JEDEC
Order Number DS90CR287MTD or DS90CR288AMTD
Dimensions shown in millimeters only
NS Package Number MTD56



64 ball, 0.8mm fine pitch ball grid array (FBGA) package
Dimensions shown in millimeters only
Order Number DS90CR287SLC or DS90CR288ASLC
NS Package Number SLC64A

Notes

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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