Increasing resolution and faster frame rates have caused cameras for machine vision systems to steadily grow in their need for bandwidth. The popular Camera Link interface, however, tops out at 850 Mbytes/second and 10G Ethernet interface can only manage 1.2 Gbytes/second, even as an increasing number of cameras become available that can send more than 1 Gbyte/sec to a frame grabber. To address this shortfall, the AIA has formed the Camera Link HS committee to develop the next generation machine vision camera to framegrabber connection standard. This development will review and improve DALSA’s HSLINK proposal as it serves the full range of camera types from 300 Mbytes/second up to 6 Gbytes/second while keeping implementation simple and costs down.

Camera Link HS is designed specifically to meet the needs of all machine vision applications and therefore carries image data, configuration data and low jitter, real time triggering signals over a simple network topology supporting cameras, intermediate devices and frame grabbers. The interface has taken the key strengths of Camera Link®, and added new features and functions to meet the customer demands of today and tomorrow. Camera Link HS is designed from a system point of view, ensuring the ability to create low cost cameras and frame grabbers, while meeting the ease of use, flexibility and data reliability demanded by end customers.

Features and Benefits of Camera Link HS

- Globally available, off-the-shelf components are used.
- Scaleable bandwidths in 300MB/s steps from 300 to 6000 Mbytes/s, 1x to 20x configurations, while maintaining a common and consistent control interface and ease of implementation.
- Camera size is minimized.
- Interface technology can be integrated into FPGAs
- Power over Camera Link HS is possible.
- Protocol handles real-time triggering. No need for a separate trigger cable.
- Real-time triggering - low jitter of 3.2ns makes Camera Link HS viable for linescan applications.
- Maintains the features of Camera Link, an industry specific connectivity solution, while employing broadly-used, off-the-shelf components with development road maps for increased performance. This protocol will have a long service life.
- Lower cost data transmission across all bandwidths.
- Reliable data transmission achieved through redundant trigger codes, hardware resend capability, and proven technology. Hardware resend enables minimal buffer sizes suitable for inclusion in FPGAs, i.e. no external memory required.
- Plug and Play - Cameras are GenICam™
- General Purpose I/O are optional and supported on the camera
- Power optimized as the number of lanes needed for data transmission scales as necessary. Friendly to the environment.
- Data Forwarding - Low cost distributed image processing is a frame grabber differentiator.
- Reference designs available to reduce implementation times.
- Designed to ensure longevity in the marketplace. Expected lifecycle is 10-20 years.
- Direct conversion to fiber optic.
- Camera Link HS Protocol - exceeding 95% video efficiency.

Functional Block Diagrams

The Camera Link HS IP Core takes in Camera Link signals and priority manages trigger, GPIO image data and configuration data and sends this information to the PHY. The IP core ensures guaranteed data delivery and simplifies design implementation in both framegrabbers and cameras. Multi-vendor PHYs that operate on 86/106, are available that serialize and de-serialize the data transmitted over the cable medium. For low bandwidth applications (<300Mbytes/s), Infiniband (IBx1) or Coax cabling offers a low cost solution. For applications up to 2100Mbytes/s, a single CX4 cable is used, which significantly reduces the size and number of cables required compared to today’s machine vision standards, and still delivers 15m transmission distances.
Camera Link HS - not just for High Speed
Camera Link HS is designed to support low bandwidth cameras as easily as it supports high bandwidth cameras.

A Camera Link HS 1x configuration supports on a single cable:
- Triggers with maximum 3.2 ns jitter
- 32 high speed control lines with maximum 200 ns jitter for frame by frame windowing or toggling of General Purpose I/O lines
- 100 MByte/s command channel to camera
- Power on the cable is proposed
- Video bandwidth above 300 MByte/sec

Camera Link HS 1x (up to 300 MByte/s) Implementation
The diagram below shows an implementation block diagram for a 1x configuration indicating that Camera Link HS can be integrated entirely into an FPGA without any external ICs. This ensures small size and low cost can be achieved.

Key Features of Camera Link HS
1. Lowest Cost Solution - off the shelf, multi-vendor components
2. Flexible Cables
3. Reliable Data Delivery
4. Industry Supported
5. Direct Fibre Optic Conversion possible

Possible Implementation using discrete serdes
The figure below is an actual size implementation of a Camera Link HS 1x camera featuring single printed circuit board construction.

Contact Name
If you have any questions or feedback on Camera Link HS, please contact: Jeff Fryman, Director, Standards Development, JFryman@robotics.org or Mike Miethig (Camera Link HS Chair), mike.miethig@dalsa.com

Camera Link HS Committee
The committee is made of camera, framegrabber and cable companies and are working towards a specification release in 2011. Currently participating in the committee are: 3M Company, ANAFOCUS, Basler, Bitflow, Components Express, Dalsa, Great River Technology, Intercon 1, Matrox, Mikrotron, National Instruments, PCO, Silicon Software, Stemmer Imaging, Toshiba Teli.